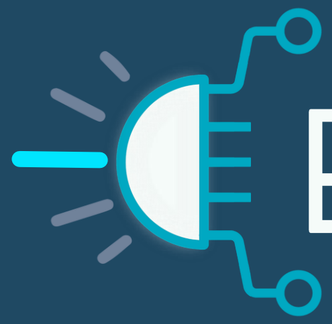

COST ACTION CA24131
European Network for radiation-detection based Research and Innovation addressing increasing societal CHallenges (ENRICH)

ENRICH

Science and Technology Facilities Council

Technology

Matt Wilson

UKRI – STFC – Rutherford Appleton Laboratory
On behalf of the Detectors & Electronics Division

Data Acquisition Systems for High Bandwidth Detectors and Real Time Processing

cost EUROPEAN COOPERATION IN SCIENCE & TECHNOLOGY

Funded by the European Union

ENRICH COST Annual Meeting, 14th of July 2026, Krakow

Content

- Motivation and Challenge
- Standardising Data Outputs
- Getting data to disk with odin_data_dpdk
- Processing data in firmware in HEXITEC MHz
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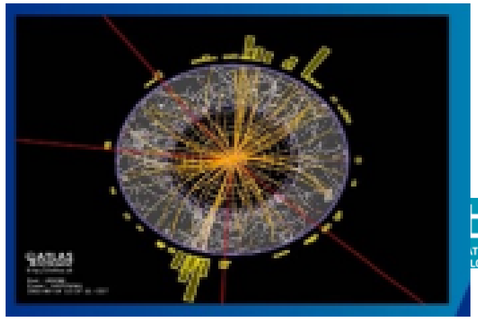
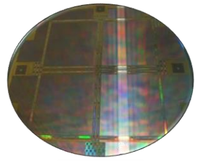
Motivation

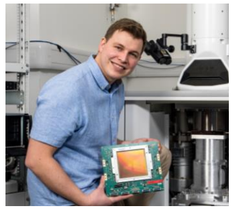
Materials - CMOS – Readout – Firmware – Software – Interconnect



Motivation



CMOS Sensors for Cryo-EM



RAL StarTracker
2003
First tests of CMOS in TEM

TEMAPS 2.0
2010
4k × 4k
18 - 40 fps
0.67G pix/s Analogue

CETA
2014
4k × 4k
40 - 50 fps

QEM
2017
4k × 4k
1000 fps @ 8 bits
~~16G pix/s Digital & LVDS~~

C100
2023
2k × 2k
2000 fps @ 12 bits
8.4G pix/s Digital & Serialisers
32G pix/s Digital & Serialisers

2008
300 keV test structure
TEMAPS

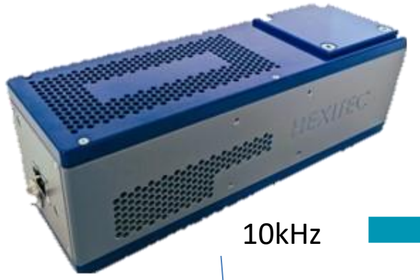
2012: FALCON I
2013: FALCON II
2015: FALCON III
FEI

2017: CETA-D
2020: CETA-S
2021: CETA-F
Thermo Fisher

2018
100 keV test structure
DEMO1

In development
4k × 4k
1900 fps @ 8 bits
Ymirion

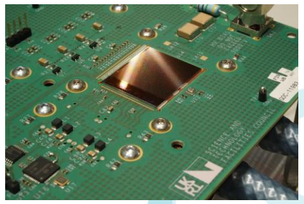
0.8Gbps out on ethernet



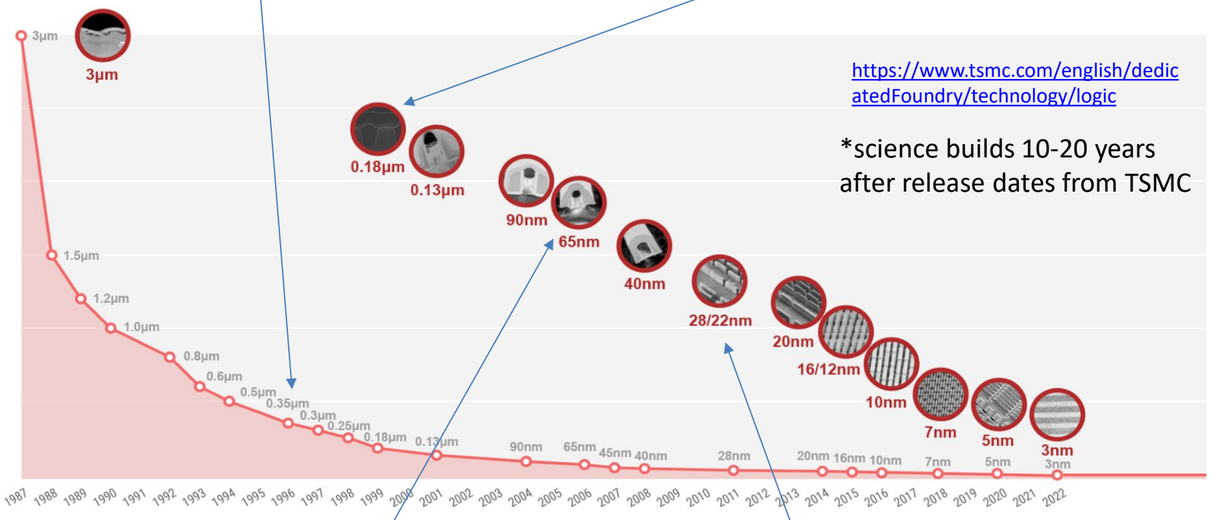
10kHz

HEXITEC Spectroscopic X-ray Imaging

20*4.1Gbps serialisers = 80Gbps

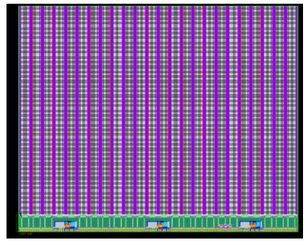


1MHz



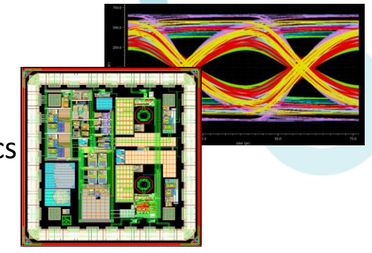
https://www.tsmc.com/english/dedicatedFoundry/technology/logic

*science builds 10-20 years after release dates from TSMC



XIDyn
4th Generation Synchrotrons
6*14.1Gbps

DRD
Next-gen particle physics
25Gbps



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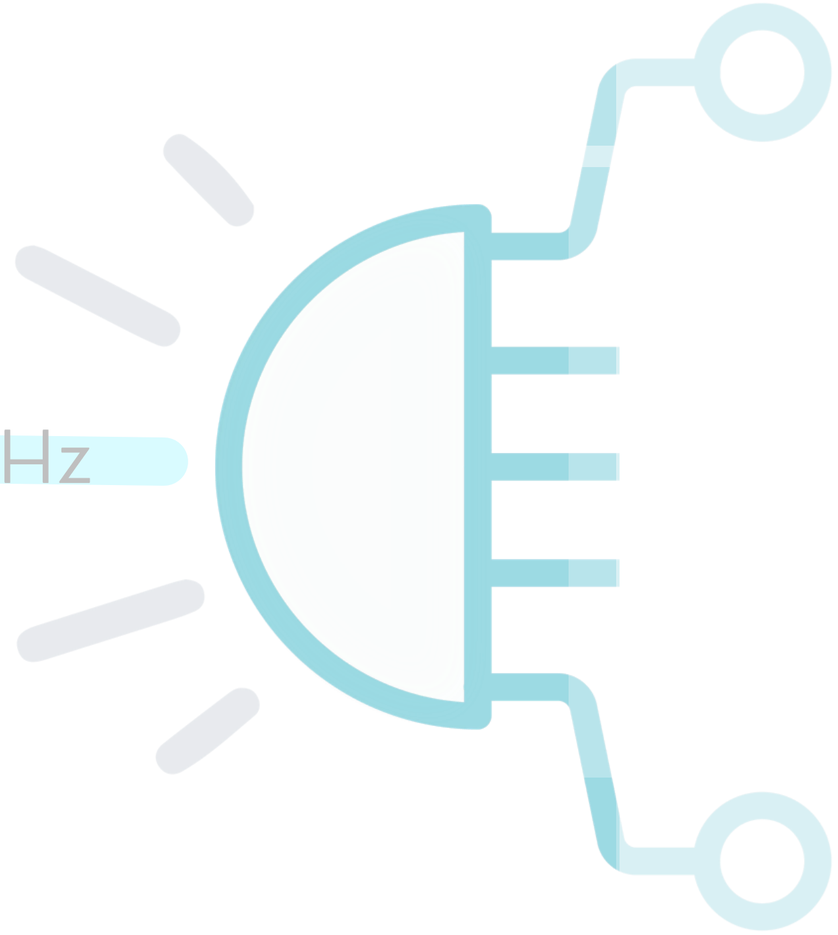
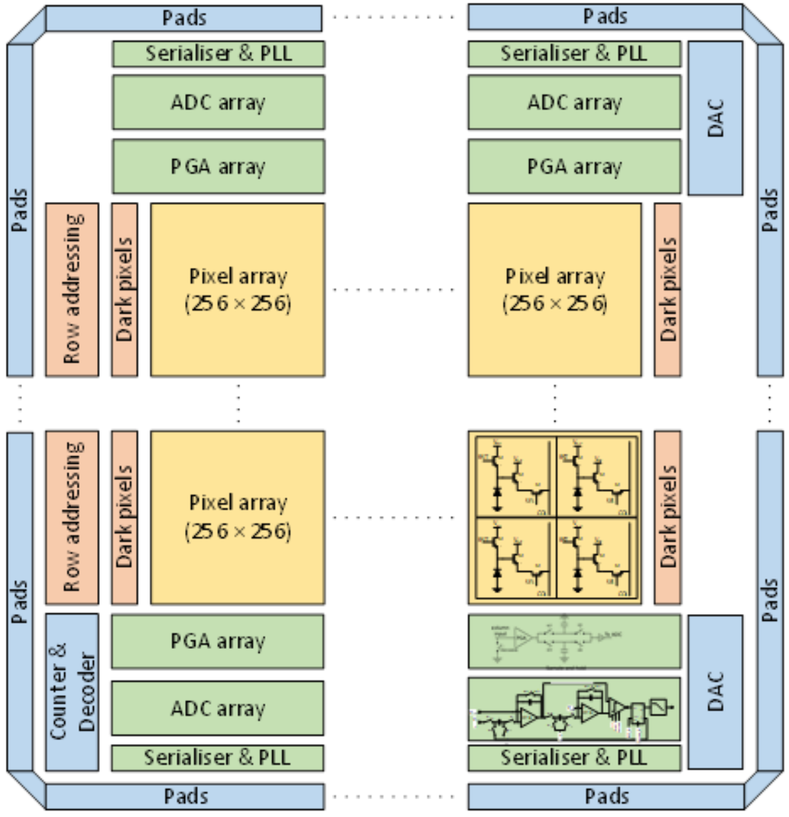
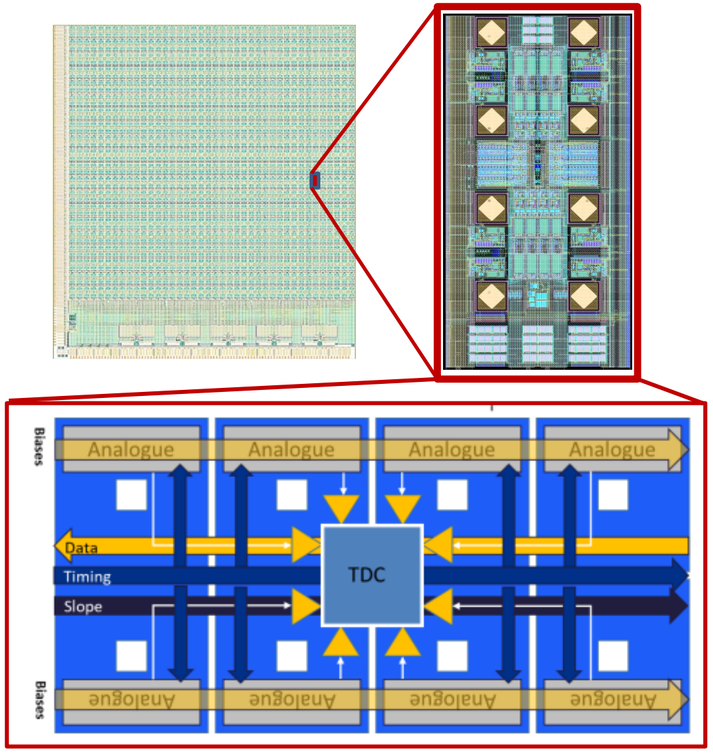


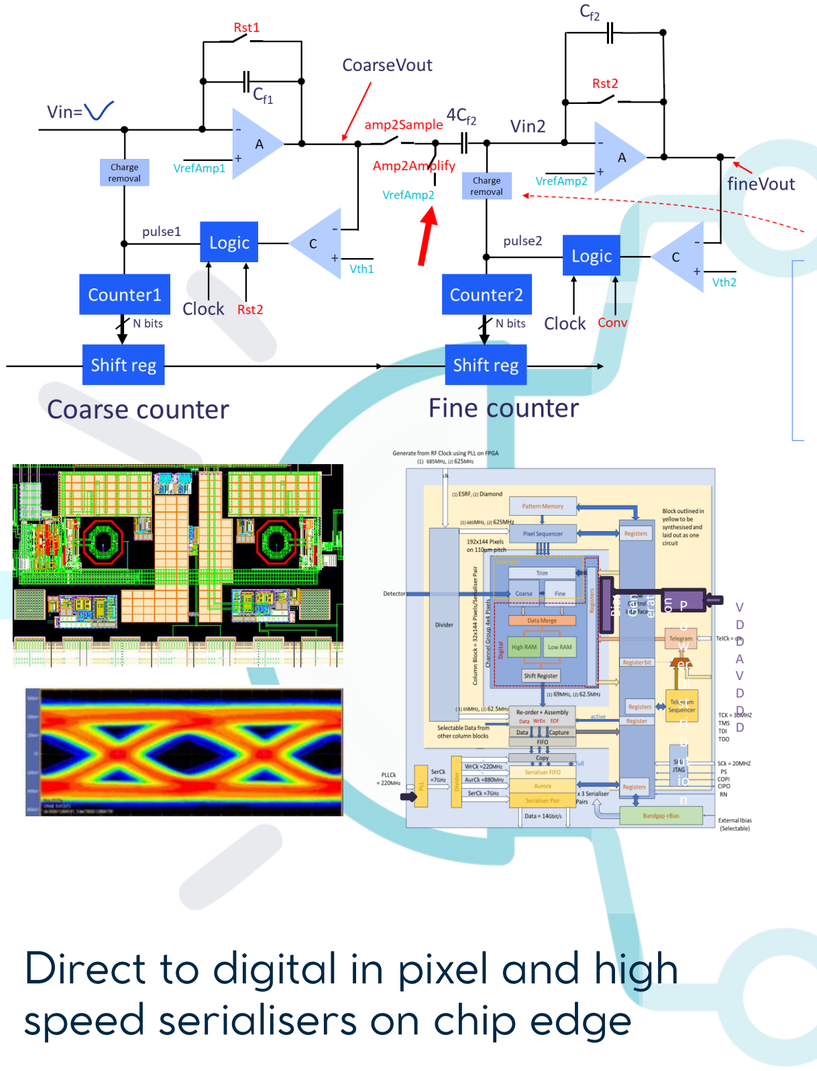
Standard Design



Column block ADCs on edge of ASIC with serialised data off chip

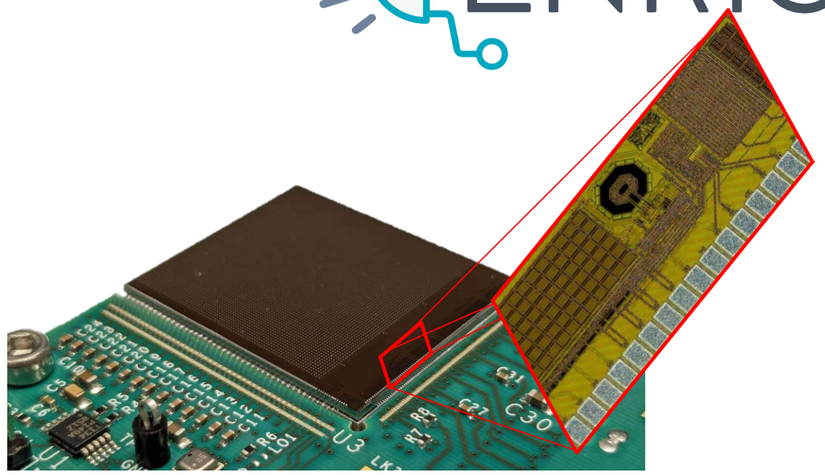


Shared digitiser in pixel groups

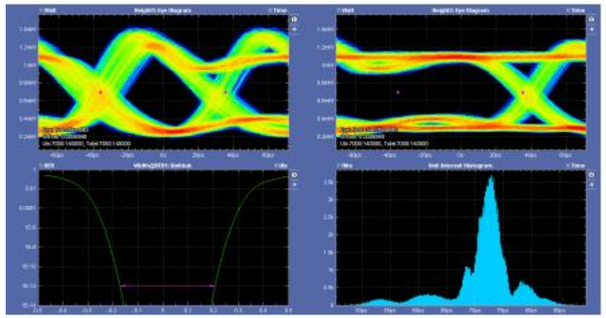


Direct to digital in pixel and high speed serialisers on chip edge

Standard Design

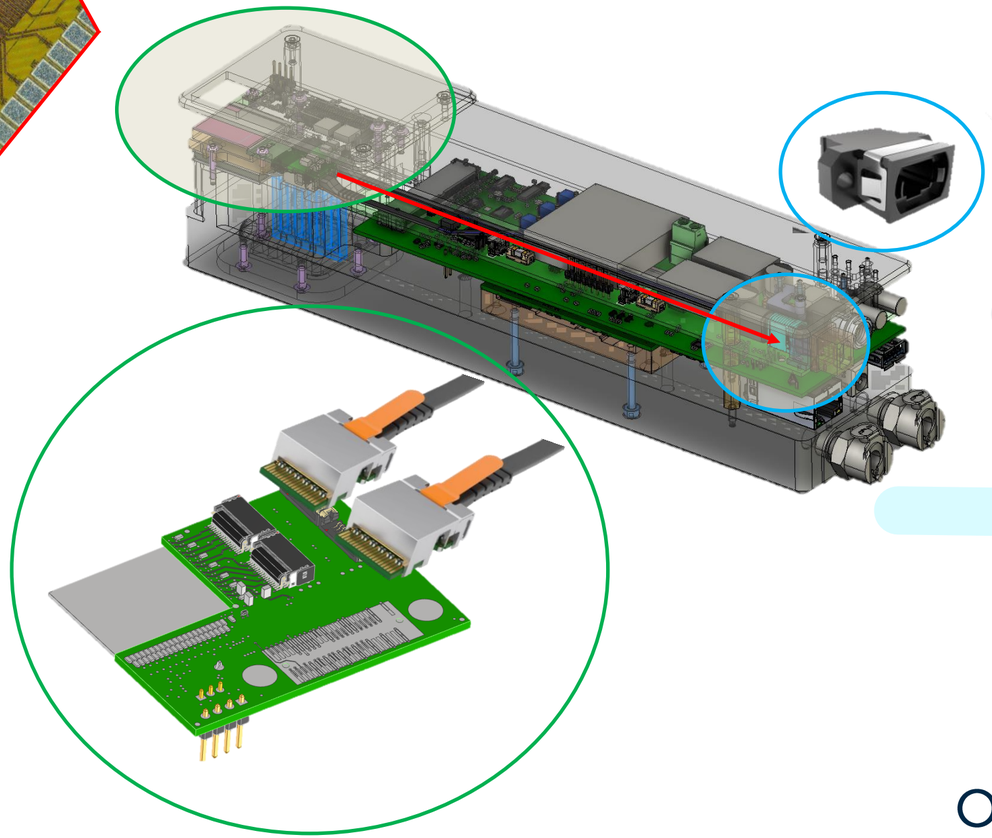


CML Gbps Serialisers



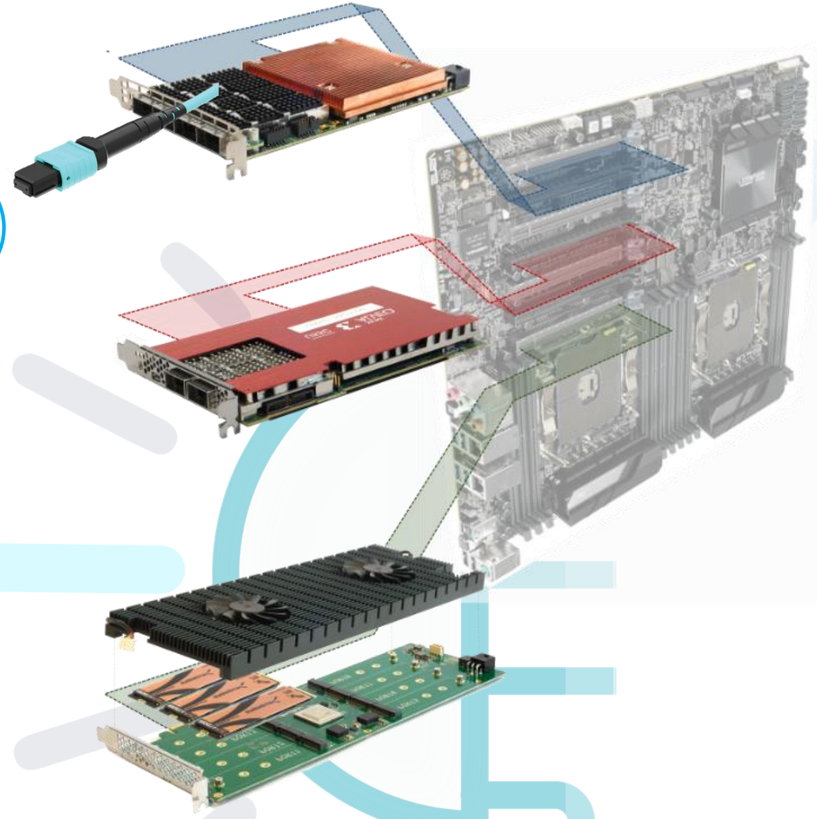
Aurora 64B/66B Protocol Specification

XILINX®



Convert to Optical ASAP

samtec



Off the shelf (or custom if needed) FPGA board to aggregate data, convert to UDP, process and store

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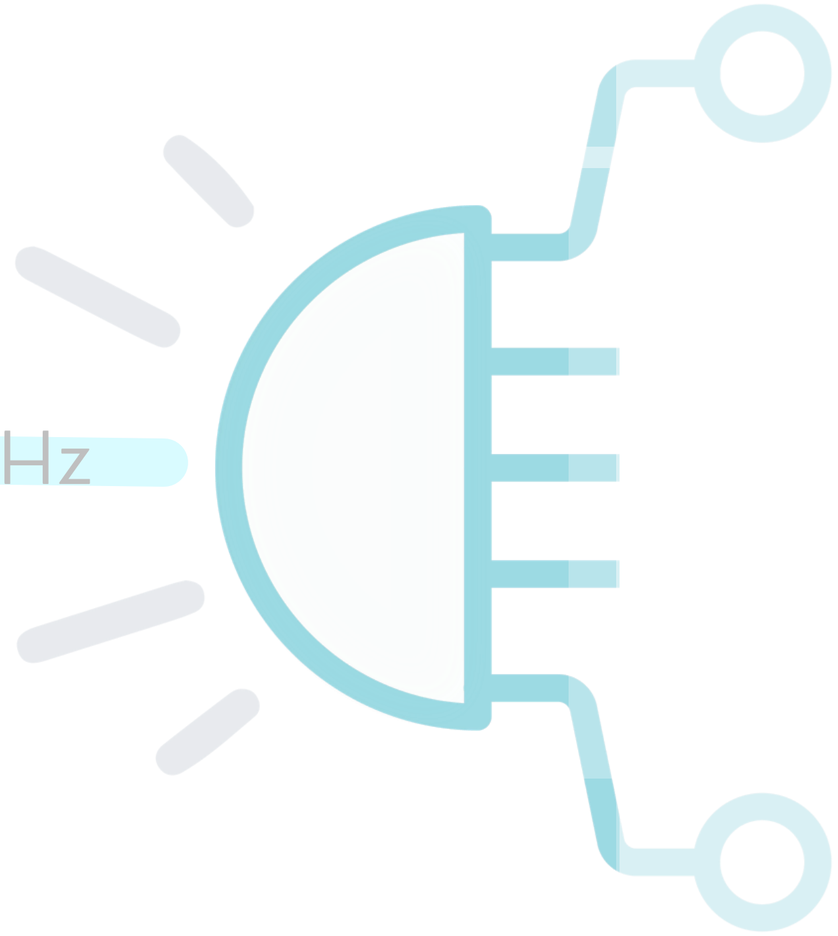
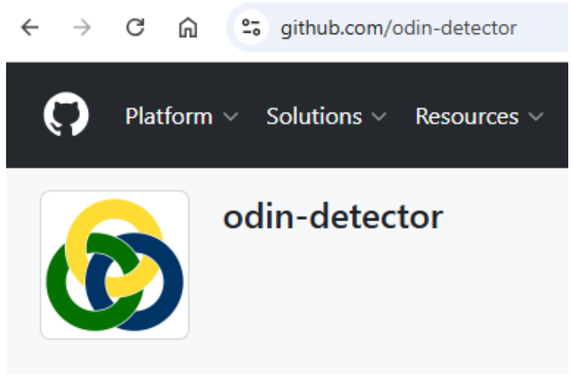
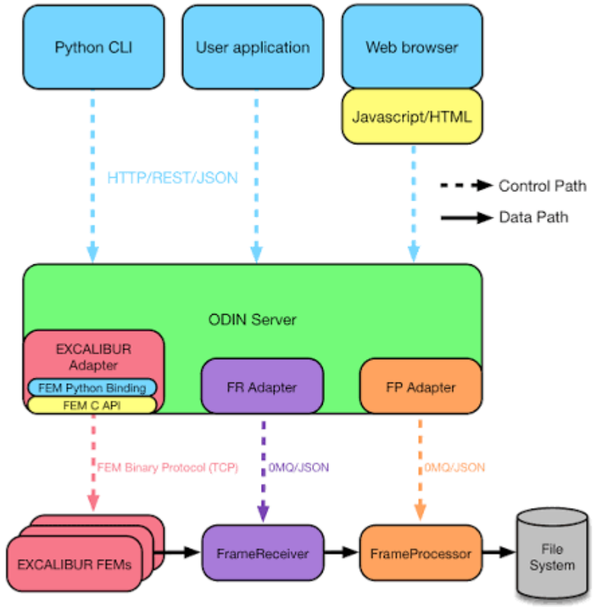


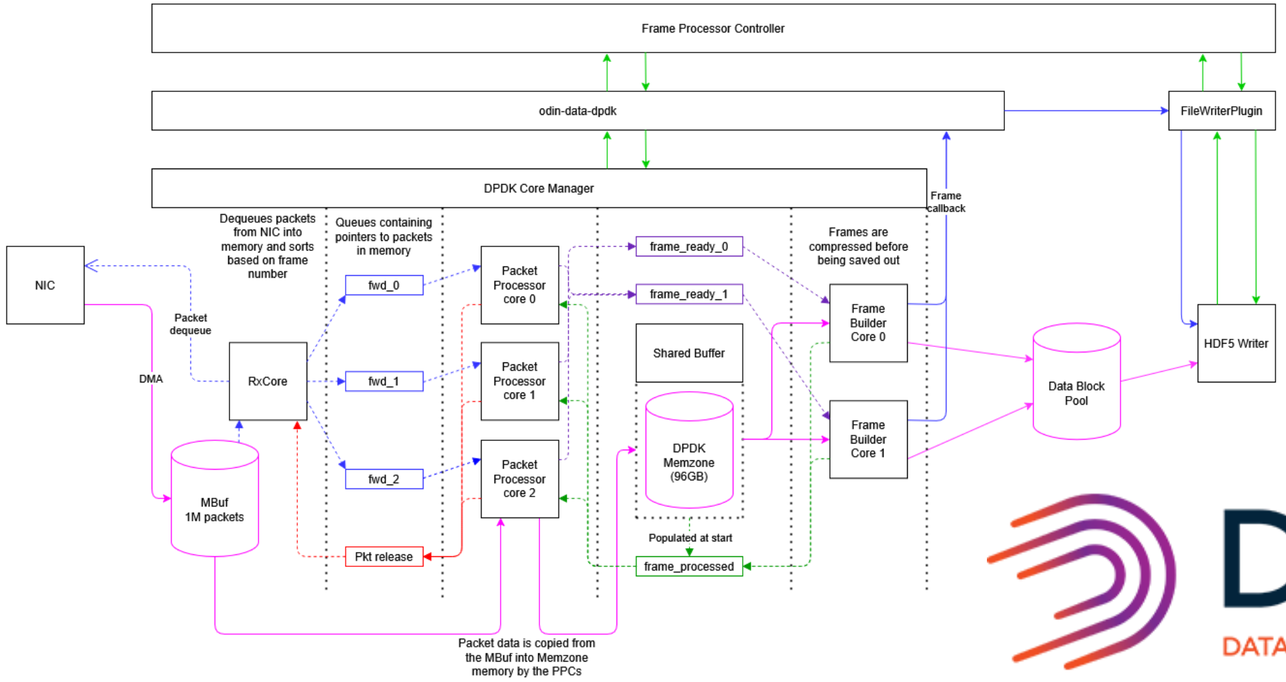
odin data dpdk





Data Plan Development Kit

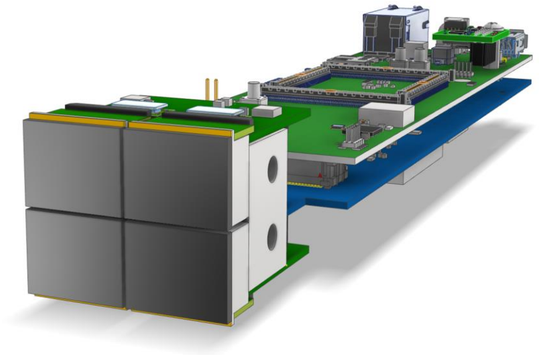
- Takes control of the Network Interface Card
  - No Linux Kernel — faster throughput
- Capture 100Gbps on a single network line
  - Stream into RAM
  - Output to .h5 files or S3 filestore



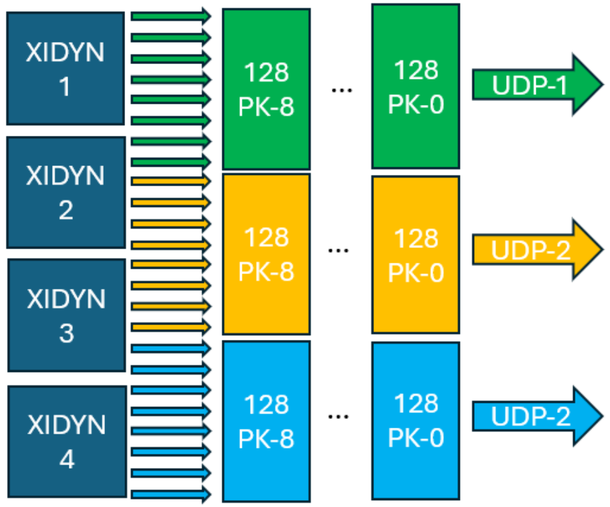
DPDK
DATA PLANE DEVELOPMENT KIT

doi:10.18429/JACoW-ICALEPCS2017-TUPHA212

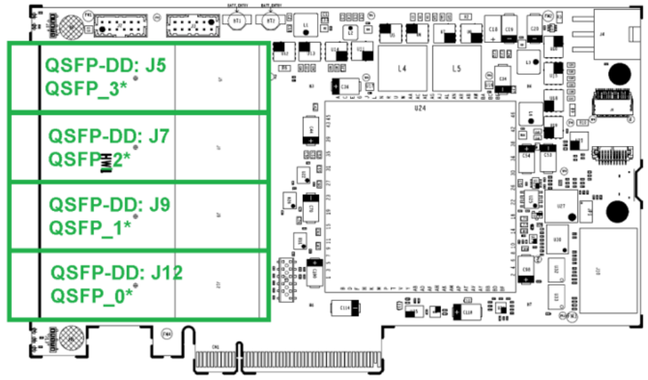
Demonstrator for XIDyn ASIC

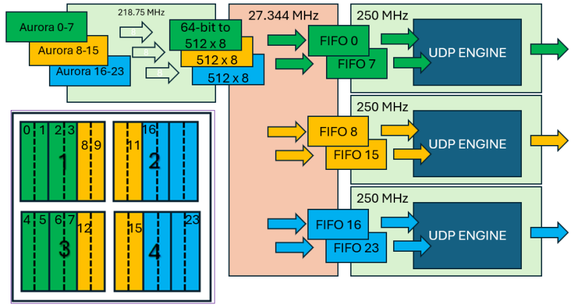


6*14.1Gbps Aurora 64b66b Outputs per ASIC → into Samtec Firefly transceivers



Alpha-data module



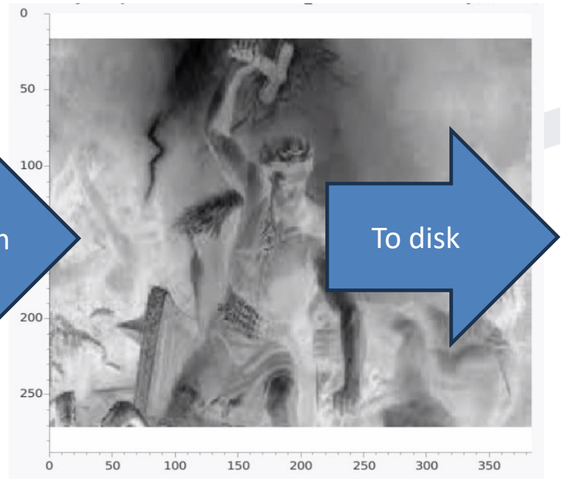


24 lanes in → 3*100Gbps UDP Out

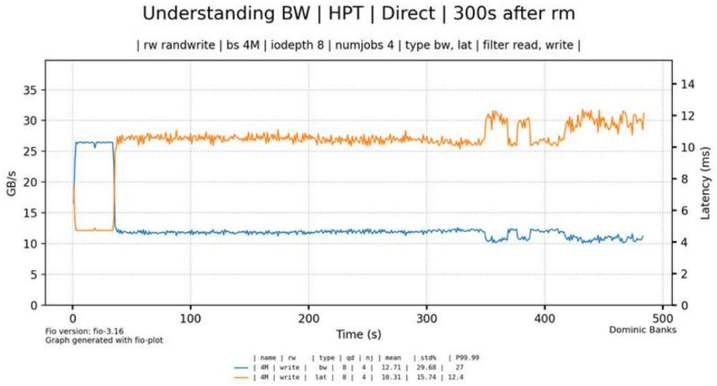
Proven with a test on the bench with FPGA emulating ASIC outputs at full speed

Receive, unpack

Pixel Ordering in FPGA



To disk



Matt.Wilson@stfc.ac.uk

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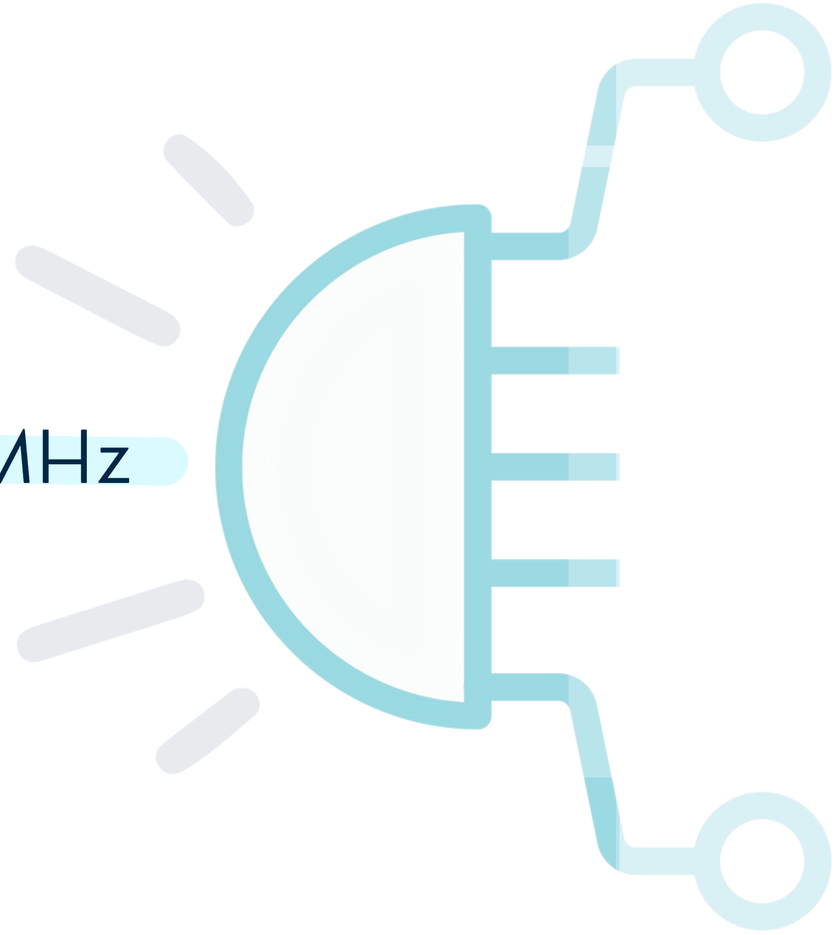
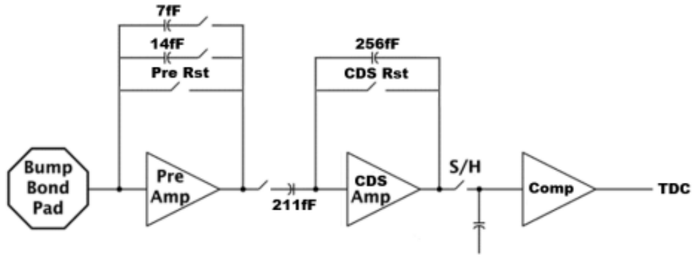


HEXITEC MHz

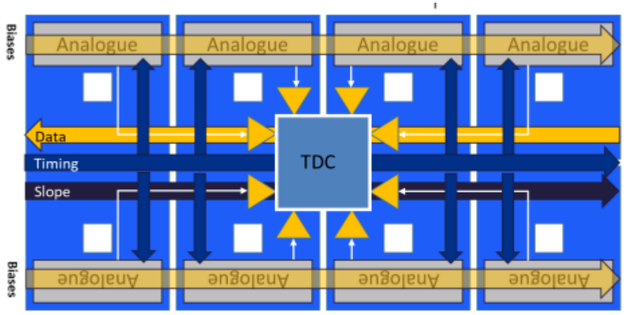
HEXITEC MHz

Parameter	Value
Pixel Pitch (mm)	250
Array Size	80 × 80
Max Frame Rate (MHz)	1.0
High Gain (keV)	2 – 100
Medium Gain (keV)	2 – 200
Low Gain (keV)	2 – 300
$FWHM_{@100keV}$ (keV)	~1
Detector Material	CdZnTe
Thickness (mm)	2

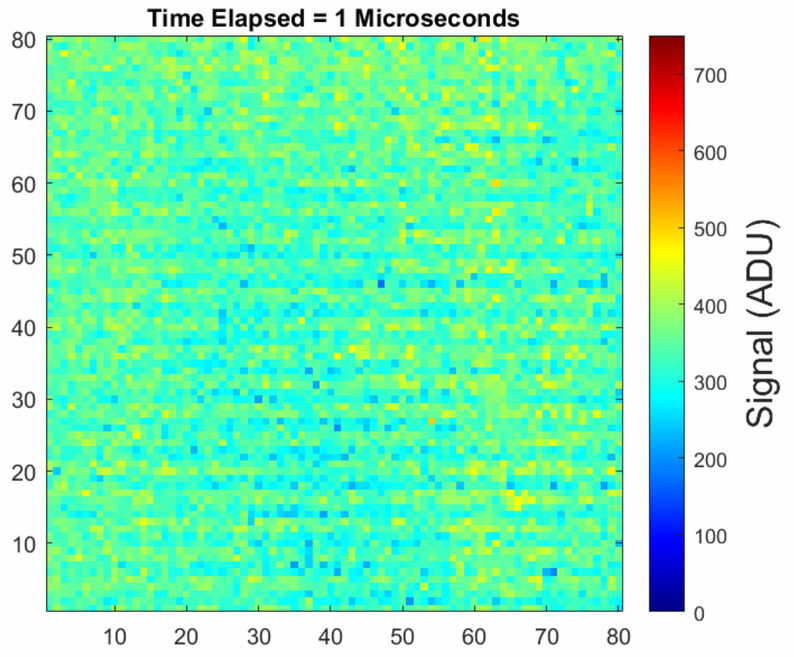
CDS integrate charge for 1µs



2x4 pixels share 12b TDC

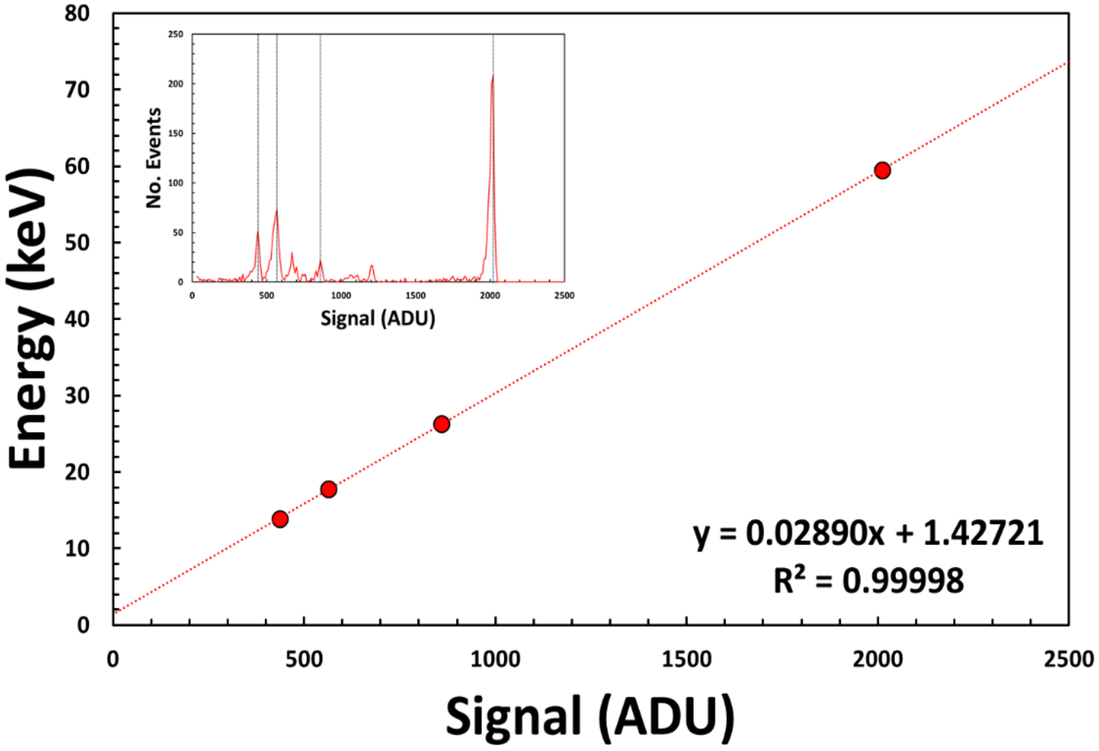


Raw Frames of Data

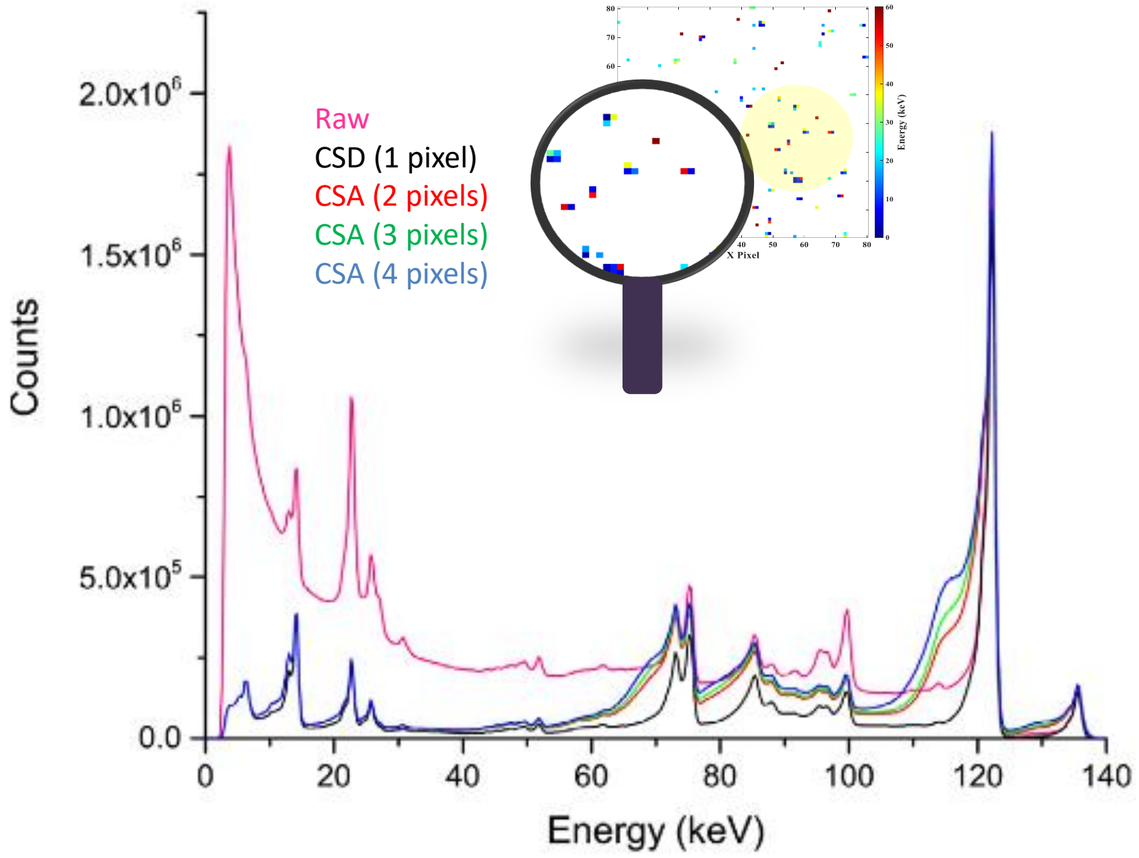


80x4 pixels into 1 of 20 4.1Gbps serialisers

HEXITEC MHz



Every pixel has to be calibrated individually – linear calibration is sufficient

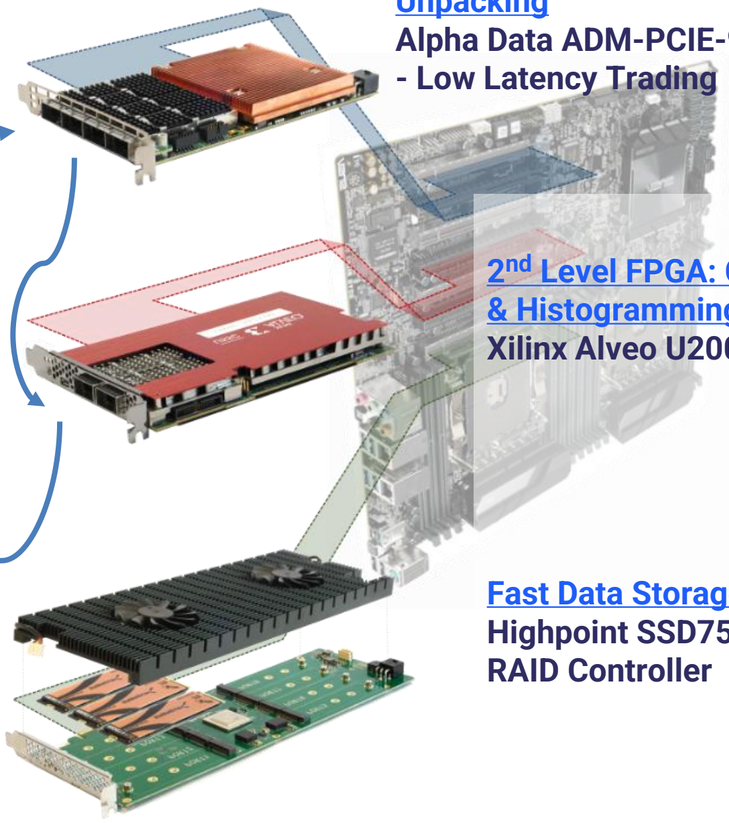


Charge Sharing for ~50% of events

HEXITEC MHz

Corrections, calibration and histogram on the fly to reduce data volume and provide tangible results

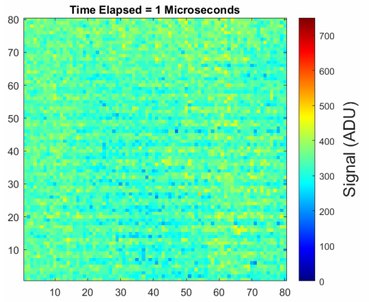
Raw data burst mode to verify and check the processing



1st Level FPGA: Data Unpacking
Alpha Data ADM-PCIE-9V5 - Low Latency Trading

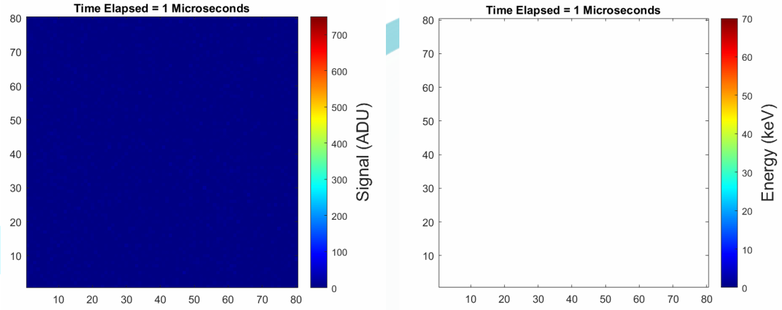
2nd Level FPGA: Correction & Histogramming
Xilinx Alveo U200

Fast Data Storage
Highpoint SSD7540 NVMe RAID Controller

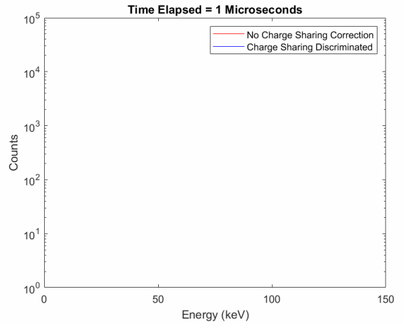


Raw Data Frames Built and Output on 100G UDP

Dark correction and Calibration on the fly



Charge sharing correction and Spectrum per pixel in FPGA and output to disk (100G UDP)



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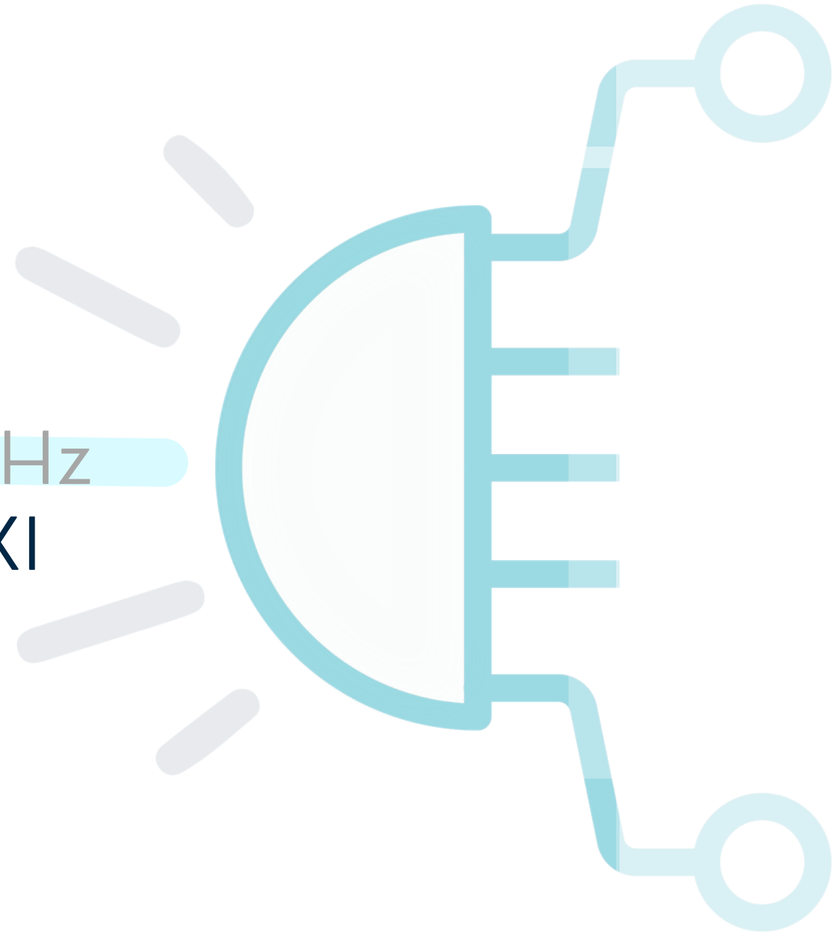
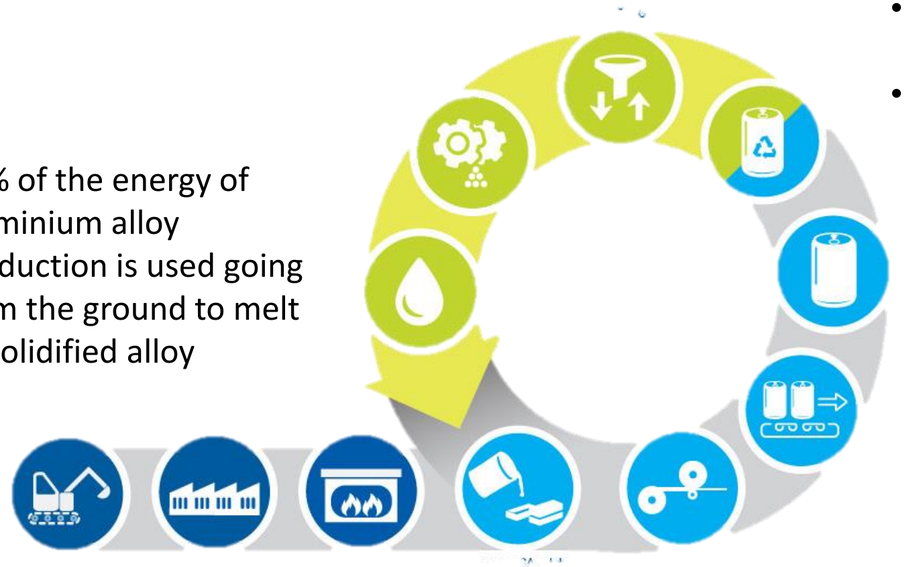
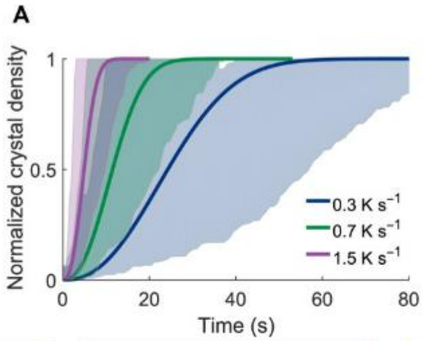


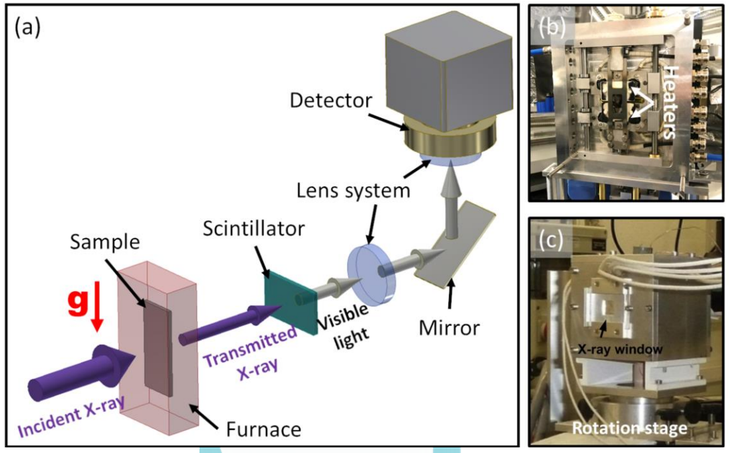
AI X-ray Imaging - AIXI

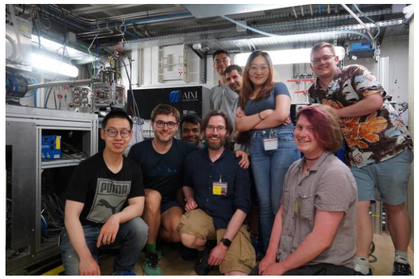
95% of the energy of aluminium alloy production is used going from the ground to melt to solidified alloy

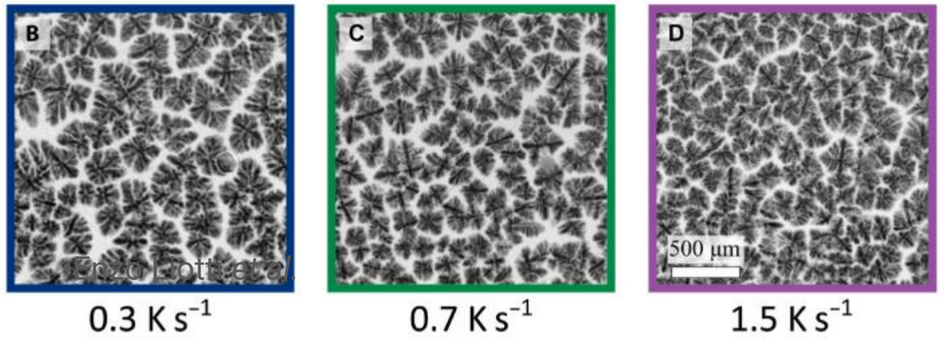


- Alloy performance dominated by the microstructure
- Difficult to recycle high performance alloys from recycled material and raw materials must be mined, processed and used
- Can we control the microstructure from the cooling rates, elemental composition, seed materials, tolerating impurities?...





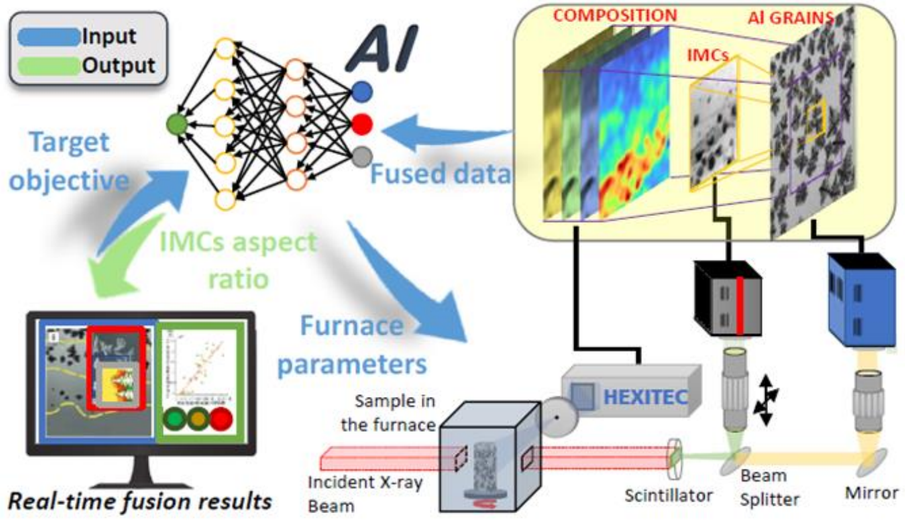


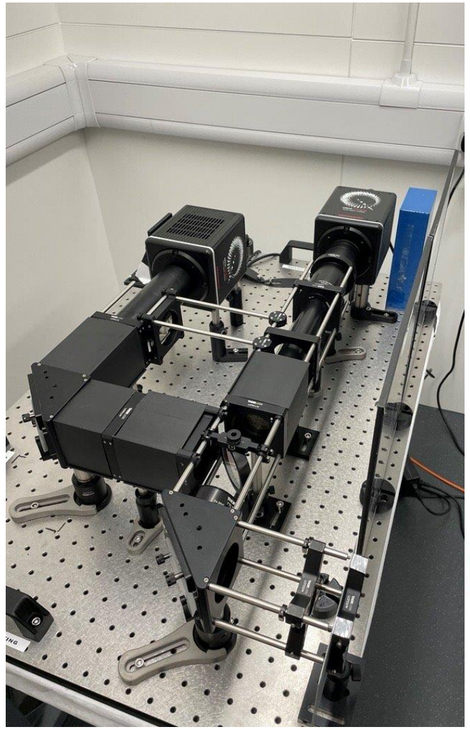


- ✓ Synchrotron imaging of metal in a furnace
- × Take TBs of data, analyse after the beamtime
- × Limited FoV at the right magnification

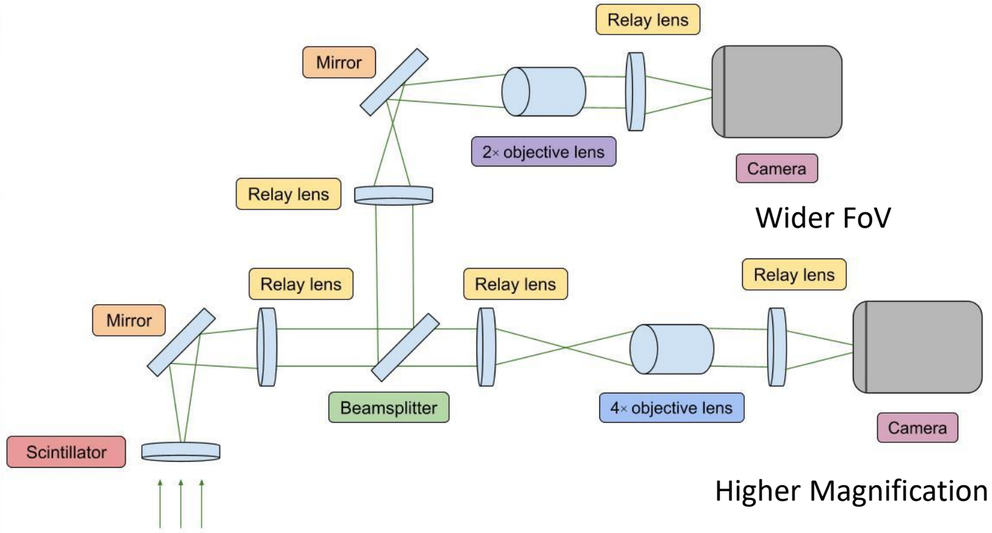
Crystal nucleation in metallic alloys using x-ray radiography and machine learning.*Sci. Adv.***4**,eaar4004(2018).DOI:10.1126/sciadv.aar4004

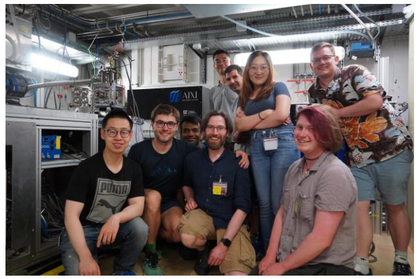
AI X-ray Imaging - AIXI





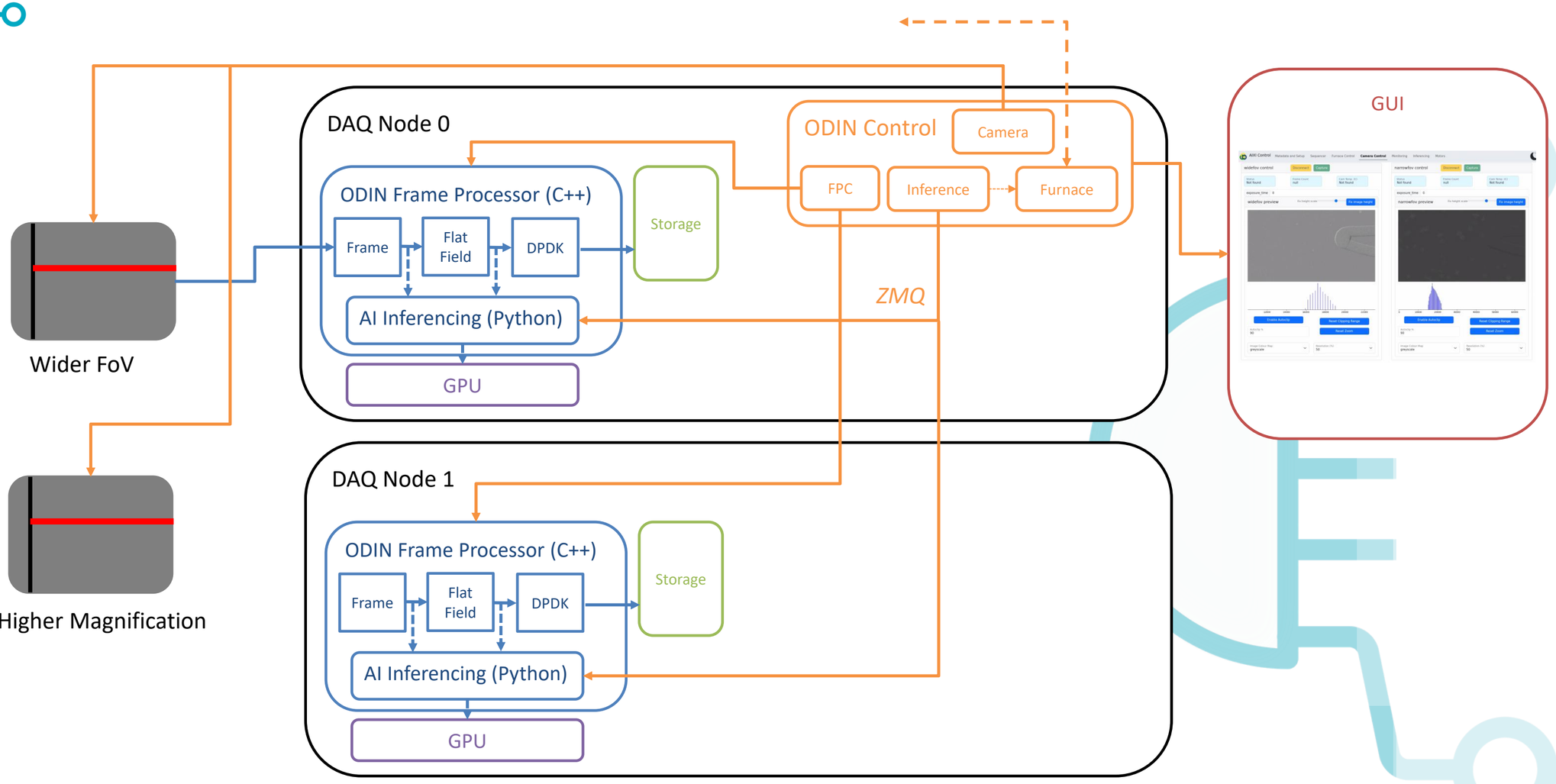
Hamamatsu qCMOS

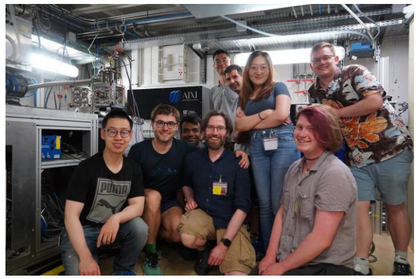




UNIVERSITY OF OXFORD
DEPARTMENT OF MATERIALS
UNIVERSITY OF SUSSEX

AI X-ray Imaging - AIXI





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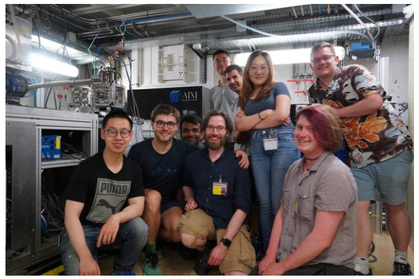
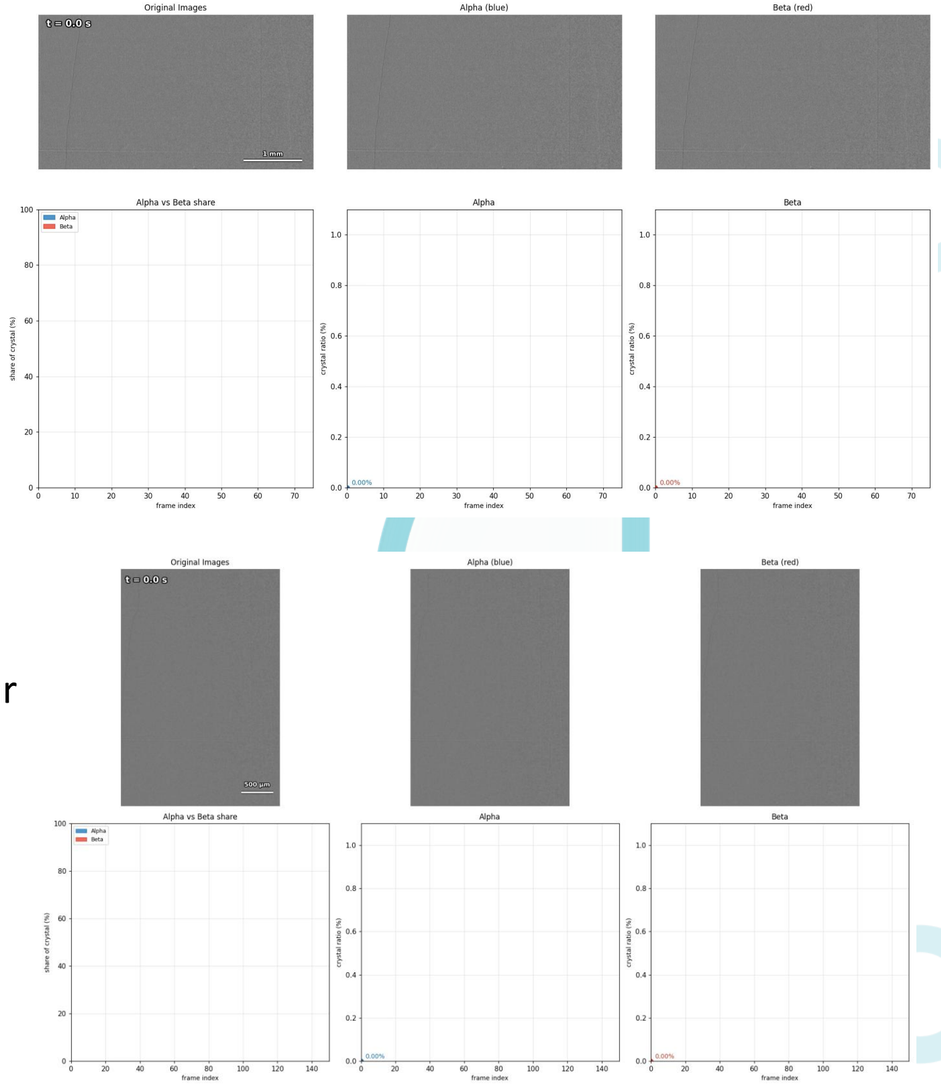
AI X-ray Imaging - AIXI

Al-Cu Alloy

- Melt phase and cooled down
- Temperature gradient to control growth upwards
- Top images are High Magnification
  - Slower frame rate as less light from optics
- Bottom images are Wide FoV to capture wider changes at the same time
- Inferencing identifying the alpha and then beta phases that form as a first example
- Measuring rates, dimensions, aspect ratios proven so far

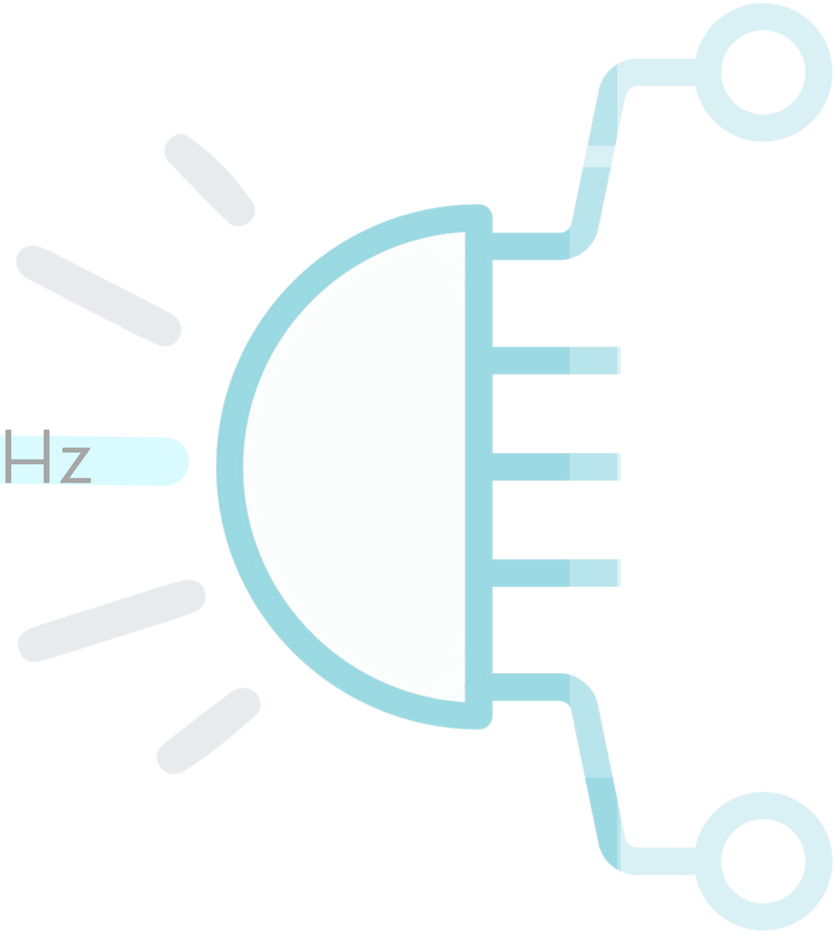




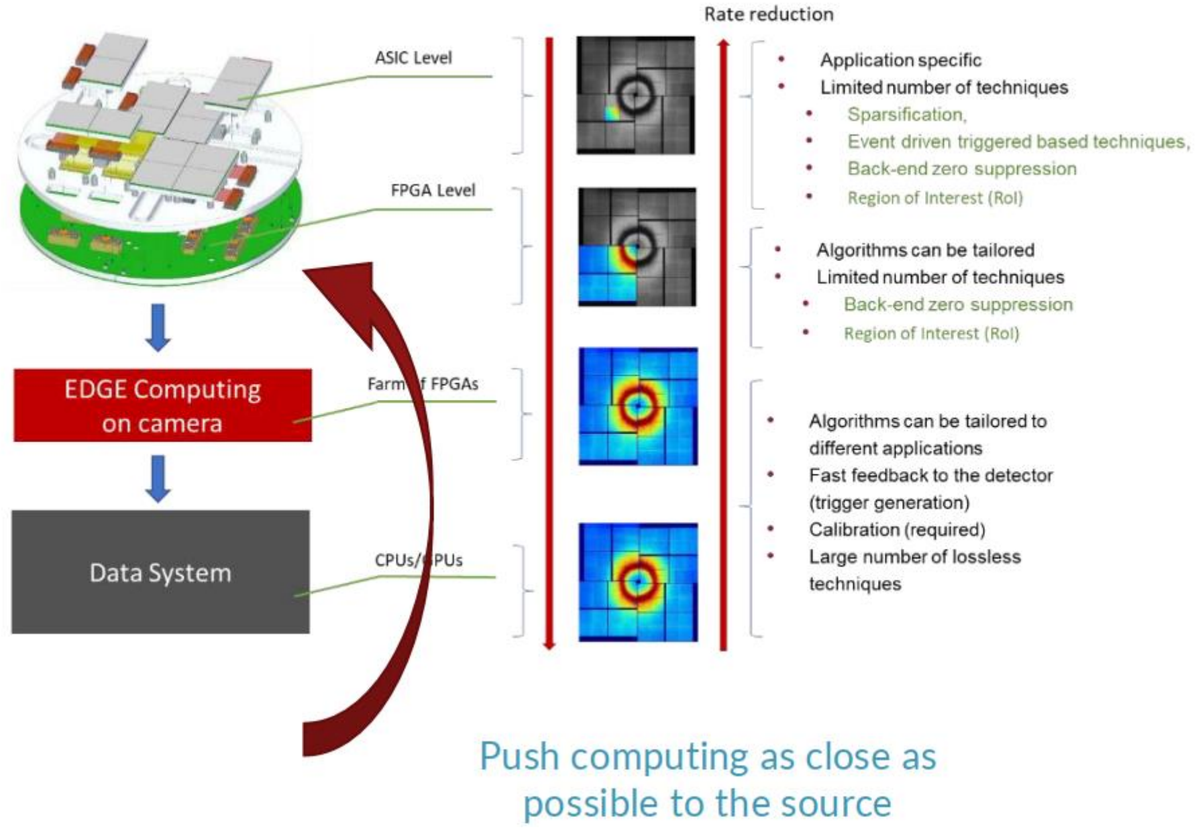
Credit: Shun Yang & Enzo Liotti, Oxford.

Content

- Motivation and Challenge
- Standardising Data Outputs
- Getting data to disk with odin_data_dpdk
- Processing data in firmware in HEXITEC MHz
- Enabling in-line AI inferencing with the AIXI Camera system



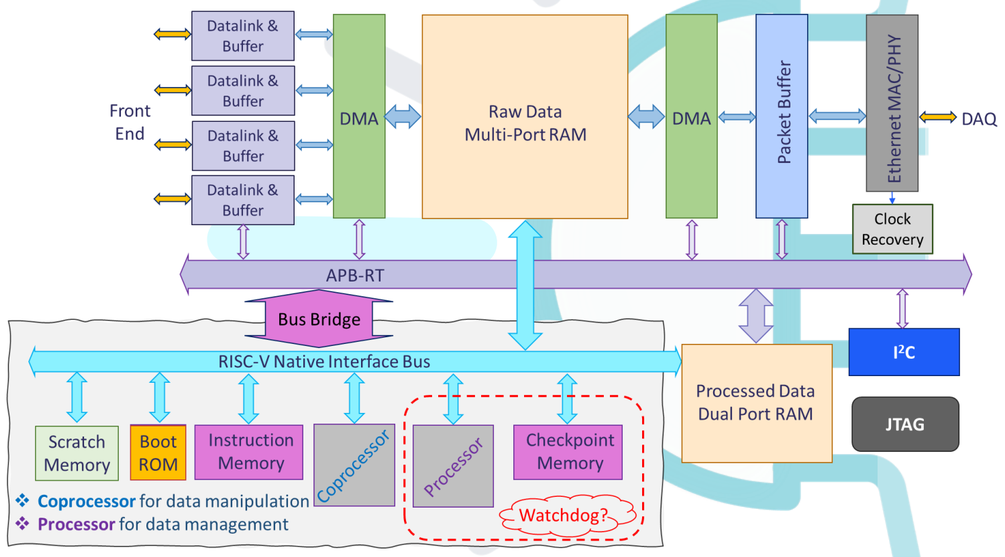
Where next?



Credit: Dionisio Doering and the team at SLAC – IFDEPS 2026

DRD7.2b: System on Chip

- **28nm MPW device**
- **Could be on an ASIC edge or a sidecar**
- **Move from Aurora to Ethernet packets**



Summary

- STFC develop and collaborate on a range of sensors and detector systems for facilities, academic partners and industrial applications
- Consistent trend of fast rates + more pixels = data deluge
- Development of re-usable IP in microelectronic, hardware, firmware and software to deploy across projects
  - Very open to share with others and take on new technology
- Examples of where and how we are using it in our collaborations
  - Providing a platform for the scientists to use it and help them extract information from raw data

Acknowledgements

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Backup Slides

- Transmission line theory (Telegrapher's equations)
  - The same basic physics for modern high-speed signal design

$$\mathbf{Z}_0 = \sqrt{\frac{R_\omega + j\omega L_\omega}{G_\omega + j\omega C_\omega}}$$