Evolution of the data acquisition and processing system in J-PET

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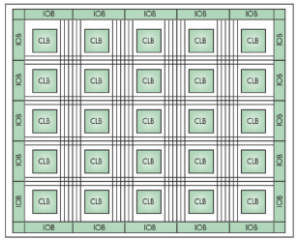
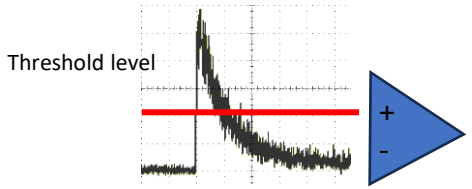
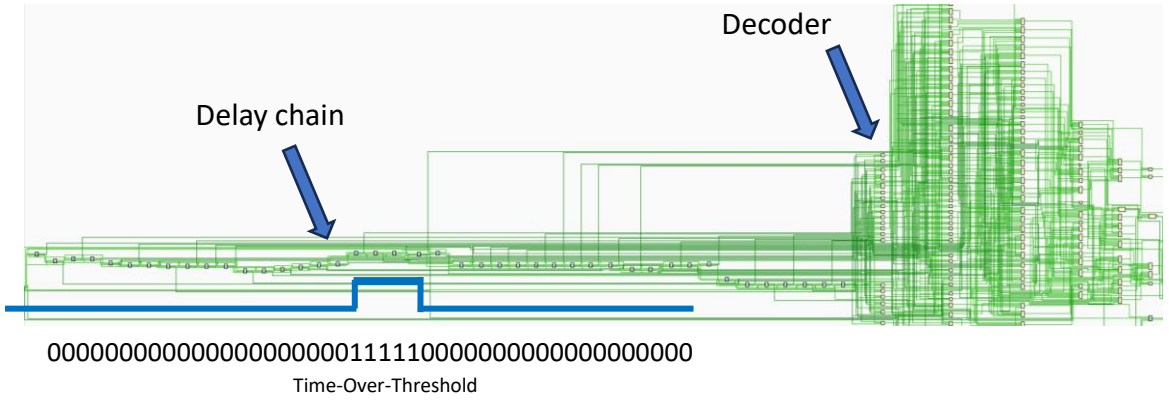
The key concepts

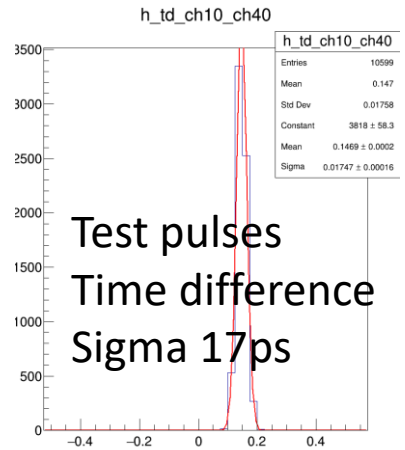
- **Field-Programmable Gate Arrays in the center of the system**
  - Reduction of the analog part
    - Analog signal discrimination and digitization with FPGA
  - Migration of functionalities into flexible FPGAs
    - Time-Digital-Converter implemented using FPGA resources
    - Data already in the chip - faster readout, less deadtime, less overhead
  - Less prone to costly mistakes and long hardware production cycles



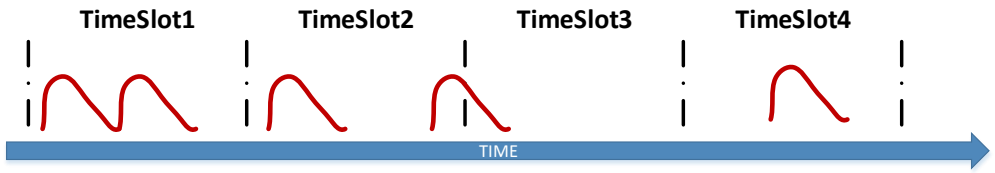
www.electronicdesign.com





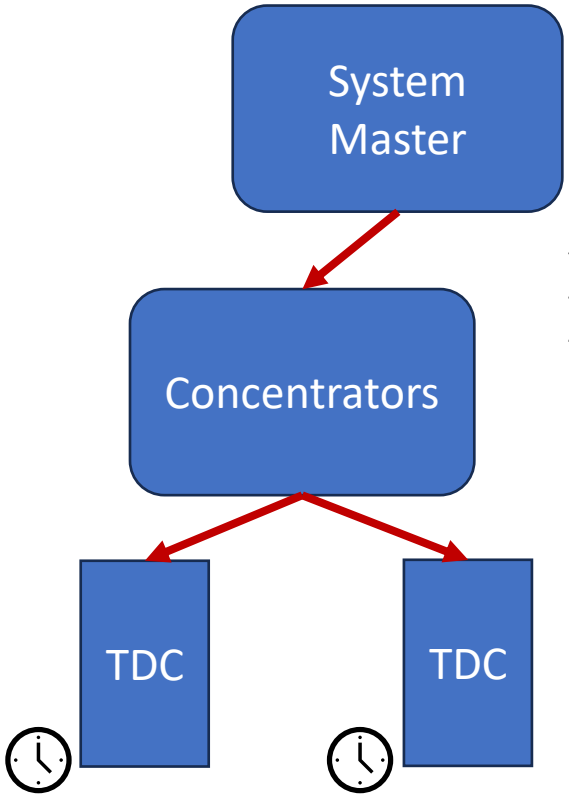


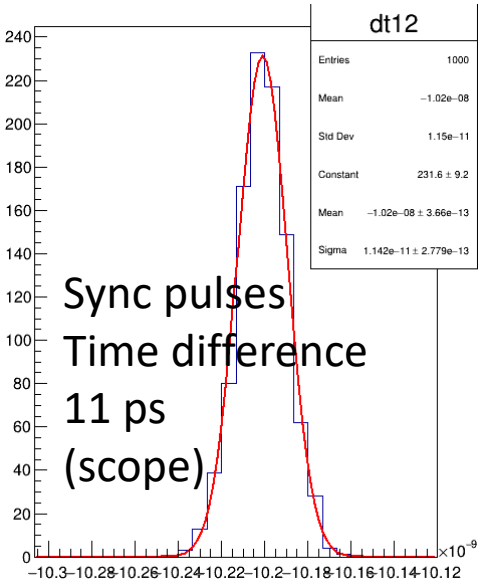
The key concepts



Korcyl G.: A system for acquisition of tomographic measurement data
Patent Application No. US 20160209522A1, 2016

- **Continuous readout**
  - No hardware trigger
    - Simplified circuits
    - Less deadtime
    - Higher throughput
  - No hardware pre-selection
    - Simplified logic
    - No artificial bias and artifacts
    - More context for deeper offline analysis
    - High level of the background
    - High data rates
  - Requires precise time synchronization
    - Common synchronization pulse on dedicated TDC channel
    - Common clock distribution





The key concepts

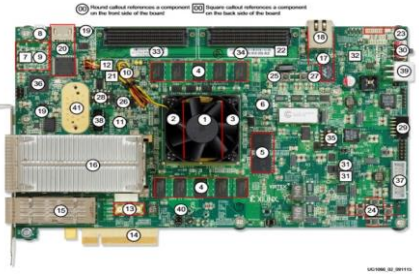
- **Apply verified standards and solutions**

  - Do not reinvent the wheel
  - Avoid common mistakes
  - Reduce development time and costs

  - Custom hardware on Front-End level only
  - Commercially available platforms on other levels
  - Standardized interfaces and protocols in Firmware
  - Industry supported IPs

VITA
Open Standards, Open Markets

FMC

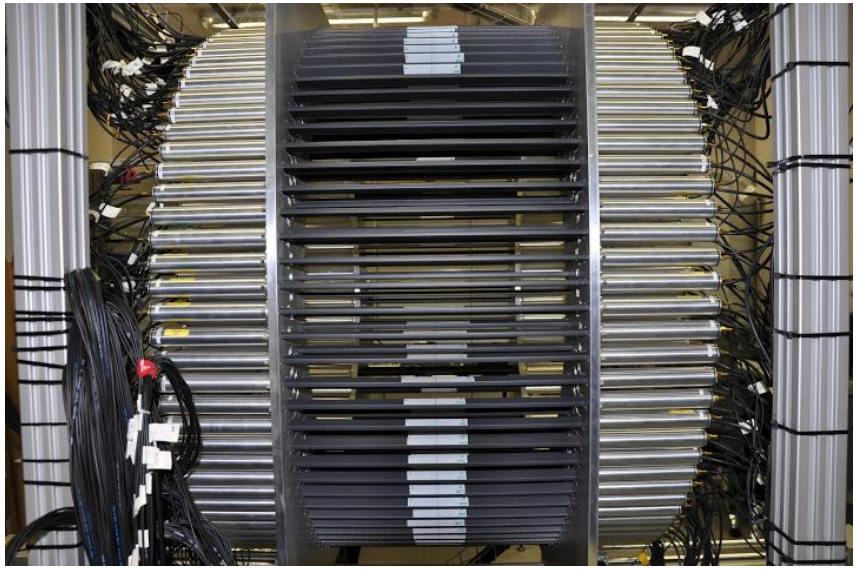


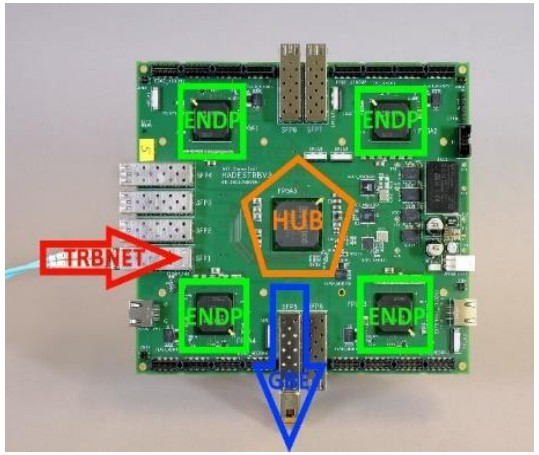
ARM AMBA
Interconnect Standards

The first J-PET system

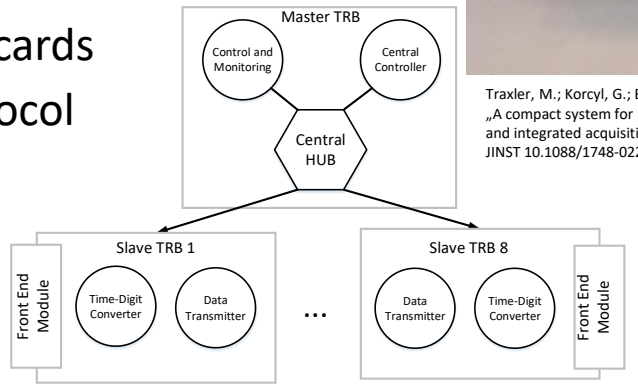
- System based on TRB platform in 2015
  - Experience from medium-scale HEP experiments
    - Jagiellonian University as part of the developers team
  - Versatile platform for complete systems
    - Over 30 hardware components
    - Complete software packages for control/monitoring, data handling
    - Verified by dozens of users in multiple experiments

- TRBv3
  - Lattice ECP3 FPGA as board controller
  - 4x Lattice ECP3 FPGA as configurable peripherals with add-on cards
  - Inter-board communication with optical links and custom protocol
  - Synchronization with dedicated LVDS lines
  - Gigabit Ethernet data output



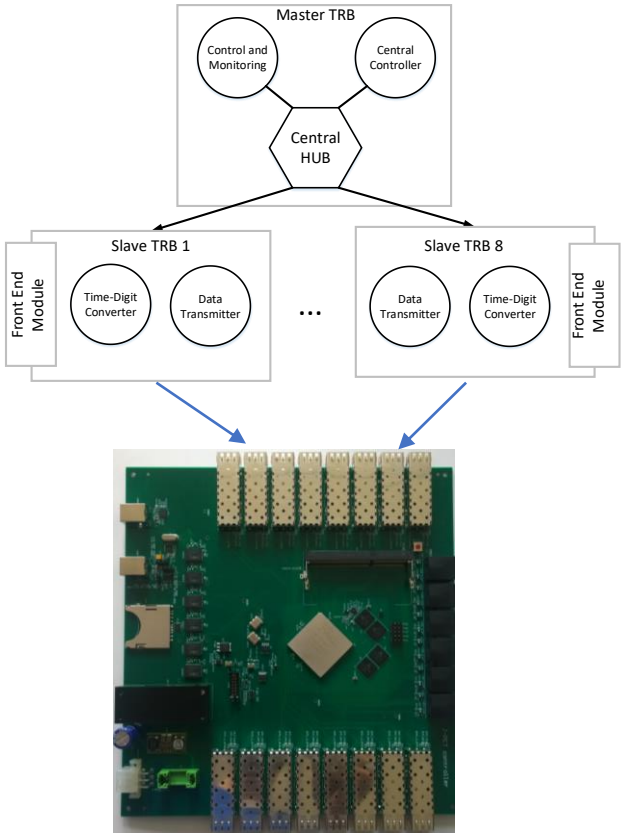


Traxler, M.; Korcyl, G.; Bayer, E.; Maier, L.; Michel, J.; Palka, M.
„A compact system for high precision time measurements (<14 ps RMS) and integrated acquisition for a large number of channels”,
JINST 10.1088/1748-0221/6/12/C12004

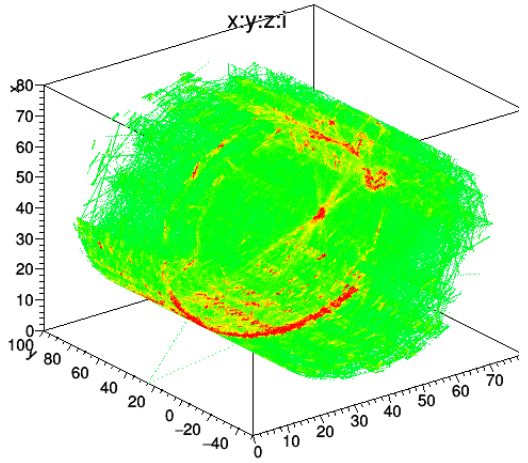


The first J-PET system

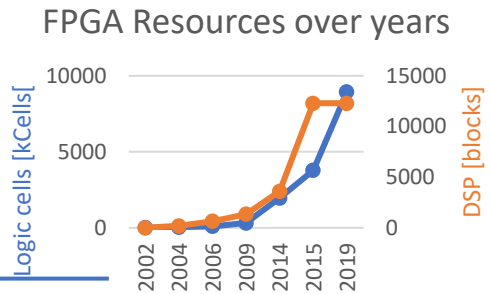
- System extended with a dedicated processing board in 2017
  - Xilinx Zynq045, 8x Ethernet inputs, 8x Ethernet outputs
  - Man-in-the-middle card
    - Online data processing (coincidences, calibrations, LOR, ROR calculation)
    - Produces live visualizations
    - Preserves original, raw data streams
    - Selectable operation mode

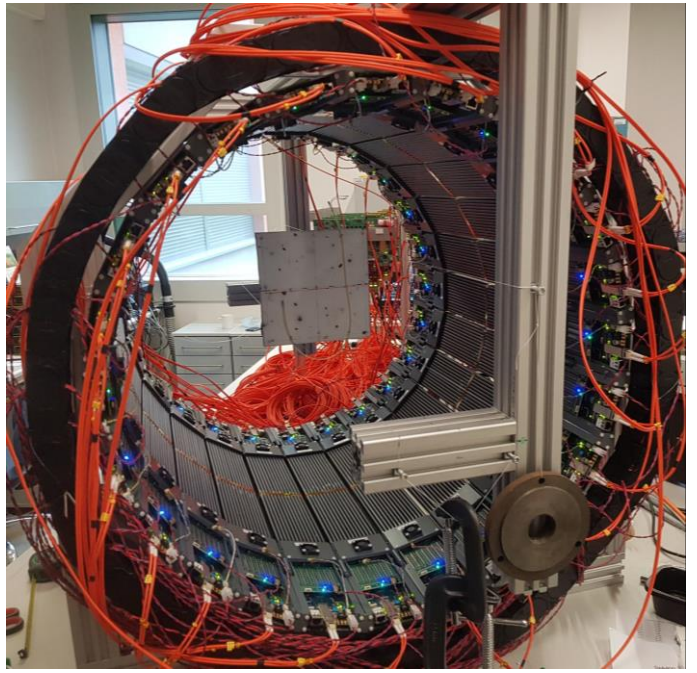


- Conclusions
  - Minimalistic FEE and signal digitization and time measurement in FPGA are satisfactory
  - Fast protocols and large throughput required for continuous readout
  - Spare logic resources required for potential pre-processing
  - TRBv3 was designed in 2011 on Lattice FPGAs, modern hardware required



The second generation

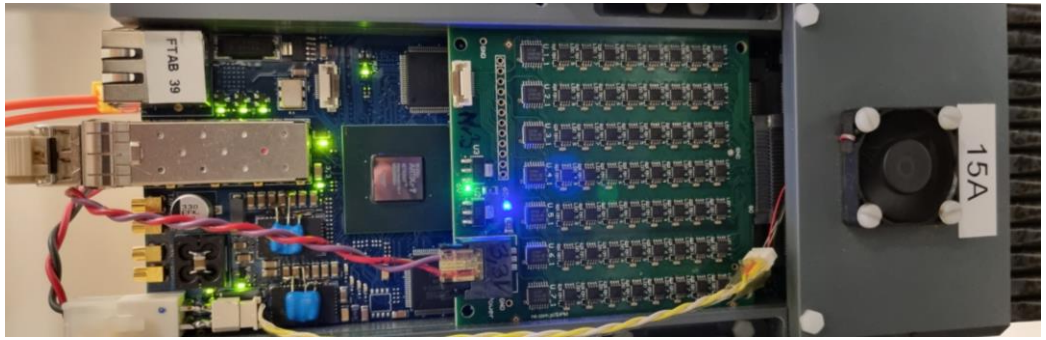


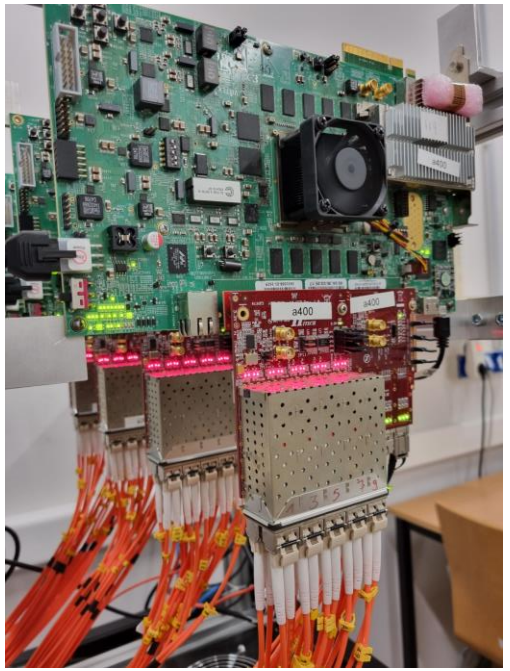


- New prototype based on silicon photomultipliers – high channel density
- Xilinx/AMD introduced efficient hardware families and dev. tools

- FEE – digitization platform redesigned
  - Artix200 as TDC and system Endpoint
- Xilinx commercial boards:
  - Virtex Ultrascale VCU108 as data concentrator
  - Zynq Ultrascale+ MPSoC ZCU102 as system controller

- 3x more analog channels – 15x more logic resources



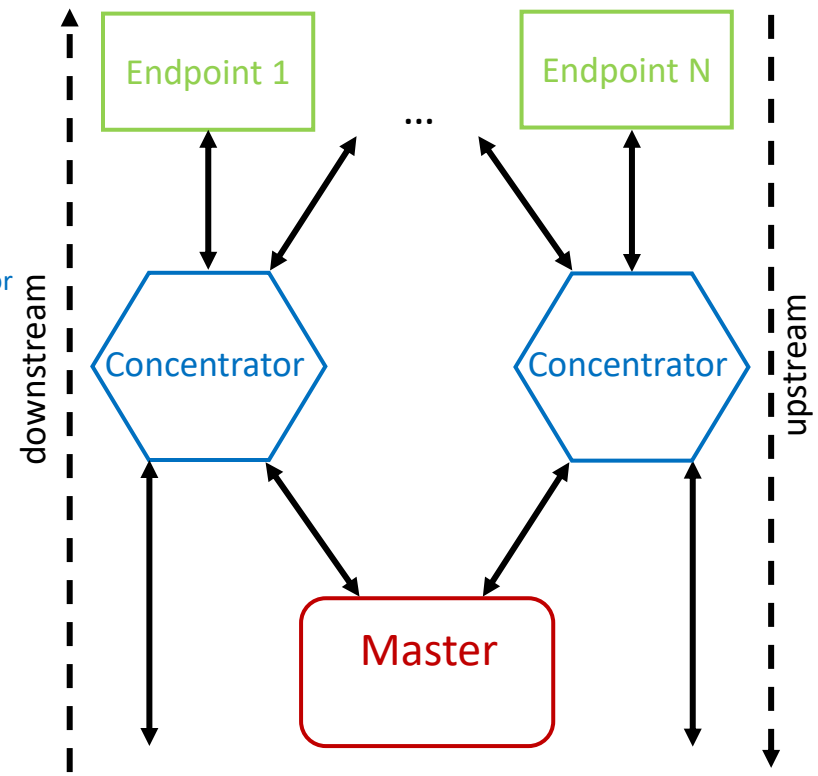


Design and development by M. Pałka

The second generation

- Efficient communication is the key
  - Downstream:
    - Precise time synchronization – synchronous links, clock distribution
    - Control/monitoring messages
  - Upstream:
    - Measurement data transport to the nearest Ethernet Gateway
  - Native Xilinx Aurora protocol
    - 5 Gbps default link speed
    - Enhanced with synchronous mode
    - Easily reusable on variety of hardware platforms
    - Easily integrable with native AXI logic interfaces

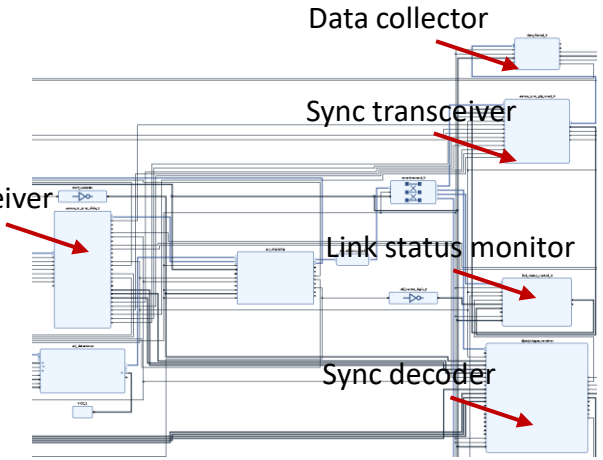
- Clock and sync pulse receiver
- Clock and sync pulse distributor
- Control/monitoring forwarder
- Data collector
- 10G Ethernet gateway



- Clock and sync pulse receiver
- Buffered data transmitter

- Source of the master clock
- Sync pulse generation
- Control/monitoring gateway

The second generation

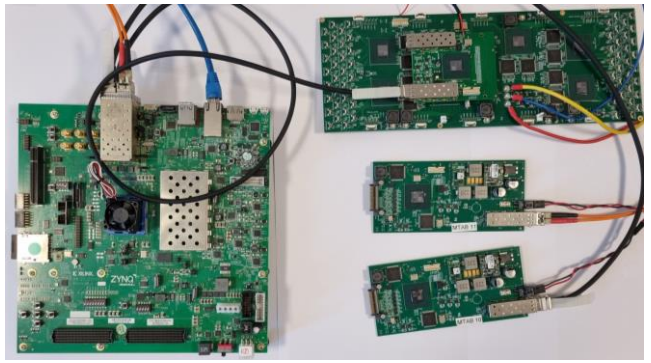


- Function within the system is defined by:
  - Hardware capabilities
  - Collection of logic function blocks
    - Sync. Transmitter/Receiver for GTP, GTX, GTH, GTY
    - Sync. decoders
    - Data collectors, forwarders
    - Time-Digit Converters
    - Control/monitoring

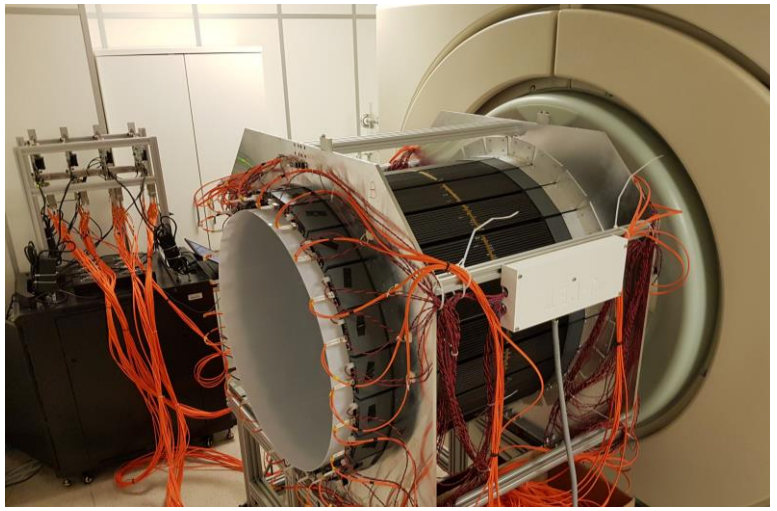
CCB IFJ PAN, Kraków 2021

- Flexible setup construction
  - Small test setups: one master and one endpoint
  - Full-scale modular J-PET
    - One master (ZCU102)
    - 4x Data Concentrators (VCU108)
    - 48x Endpoints (MTAB, FTAB)

- Complemented with an easy to use Python software package



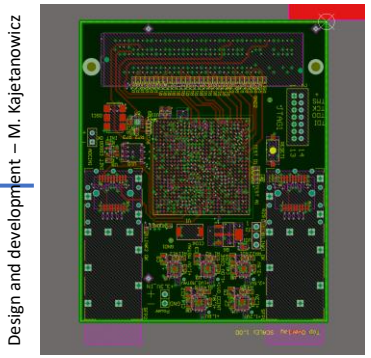
Lab setup, Kraków 2023



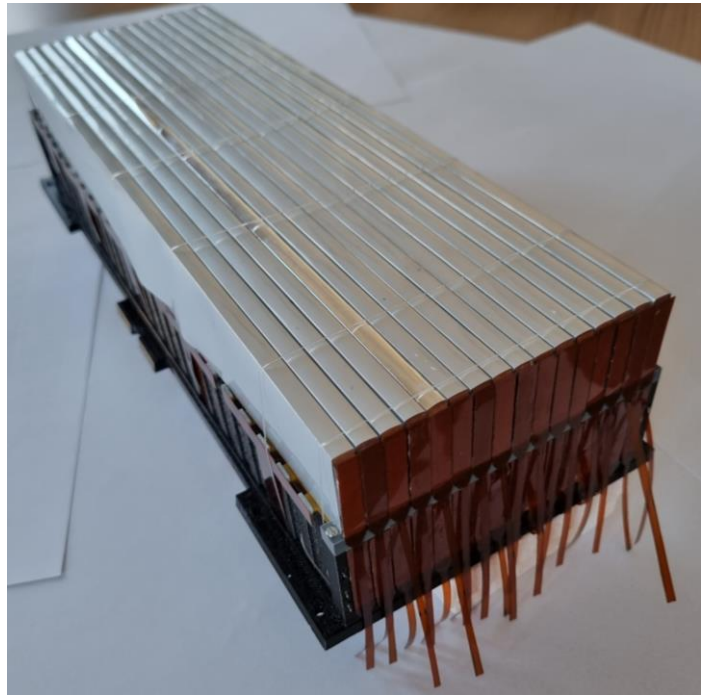
Hospital Banacha, Warsaw 2022

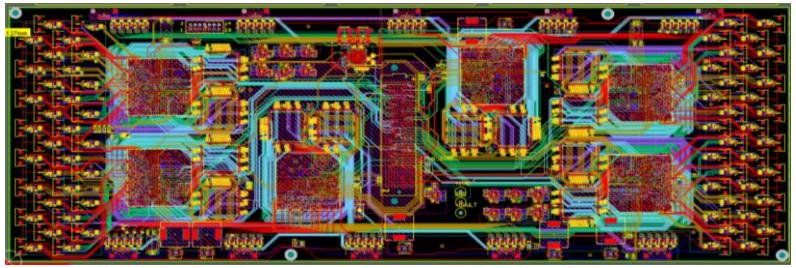
Total-Body DAQ module

- Compact with high channel density
  - Single board for an entire module
  - TDC section:
    - 356x TDC channels on 6x Artix200 FPGA (Endpoints)
    - 10x DACs for threshold setting and SiPM tuning
    - Analog signal amplifiers
  - HUB section:
    - 1x Artix200 FPGA as Concentrator
    - 2x general purpose optical links
  - Data from the entire module in a single FPGA
    - Complex online pre-processing capability

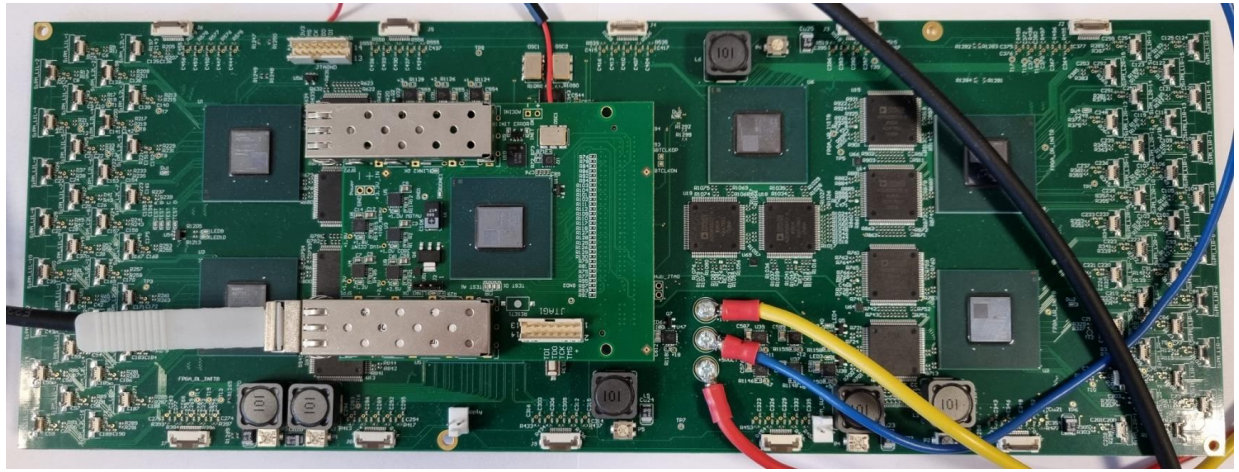


Design and development – M. Kajetanowicz





Design and development – M. Kajetanowicz



Summary

- Over 10 years of electronics, firmware and software design, development and implementation
- A versatile and flexible DAQ system for recent and future J-PET projects
  - Based on stable and verified components (HW, standards, protocols)
  - Functional backbone (time sync, data collection, control/monitoring)
  - Precise time measurement in distributed setups
  - Exchangeable Endpoints for future upgrades or adaptations
  - Expandable with data pre-processing logic cores

The DAQ group:

- Actual members:
  - Marcin Kajetanowicz
  - Piotr Kapusta
  - Wojciech Migdał
  - Szymon Niedźwiecki
  - Grzegorz Korcyl
- Former members:
  - Paweł Strzempek
  - Tomasz Bednarski
  - Marek Pałka
  - Karol Farbaniec
  - Maciej Bakalarek