FTAB - small form factor and versatile board for J-PET detector

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FTAB Architectural prerequisities

- J-PET modular design - cope with 13 scintillators
- 4 SiPM signals from each scintillator side - in total 52 SiPM analogue signals
- signals are passively split into two - 104 measurement channels
- individual thresholds
- measure time of signal arrival and its end, at the threshold level, with a very high precision $\sim$ 30ps RMS
- very compact design to place FTAB directly on the detector to avoid cumbersome cabling
- 5W of power consumption
- low voltage ripple on the power supply - maximize TDC precision and lower overall noise
- large data throughput - minimize FTAB dead time

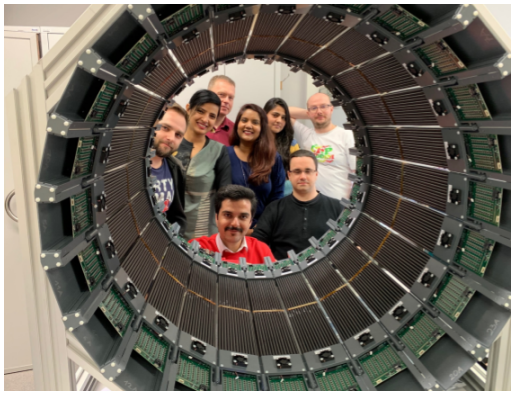

Fig. 1: J-PET detector - new concept

- only $22.5cm^2$ incorporates 52 amplifiers and 13 connectors
- to minimize size and power consumption a standard MMIC amplifiers are used: ON Semiconductors SMA-3107
- 1W of power consumption - 19mW per amplifier
- temperature is $\sim$ 37 degrees

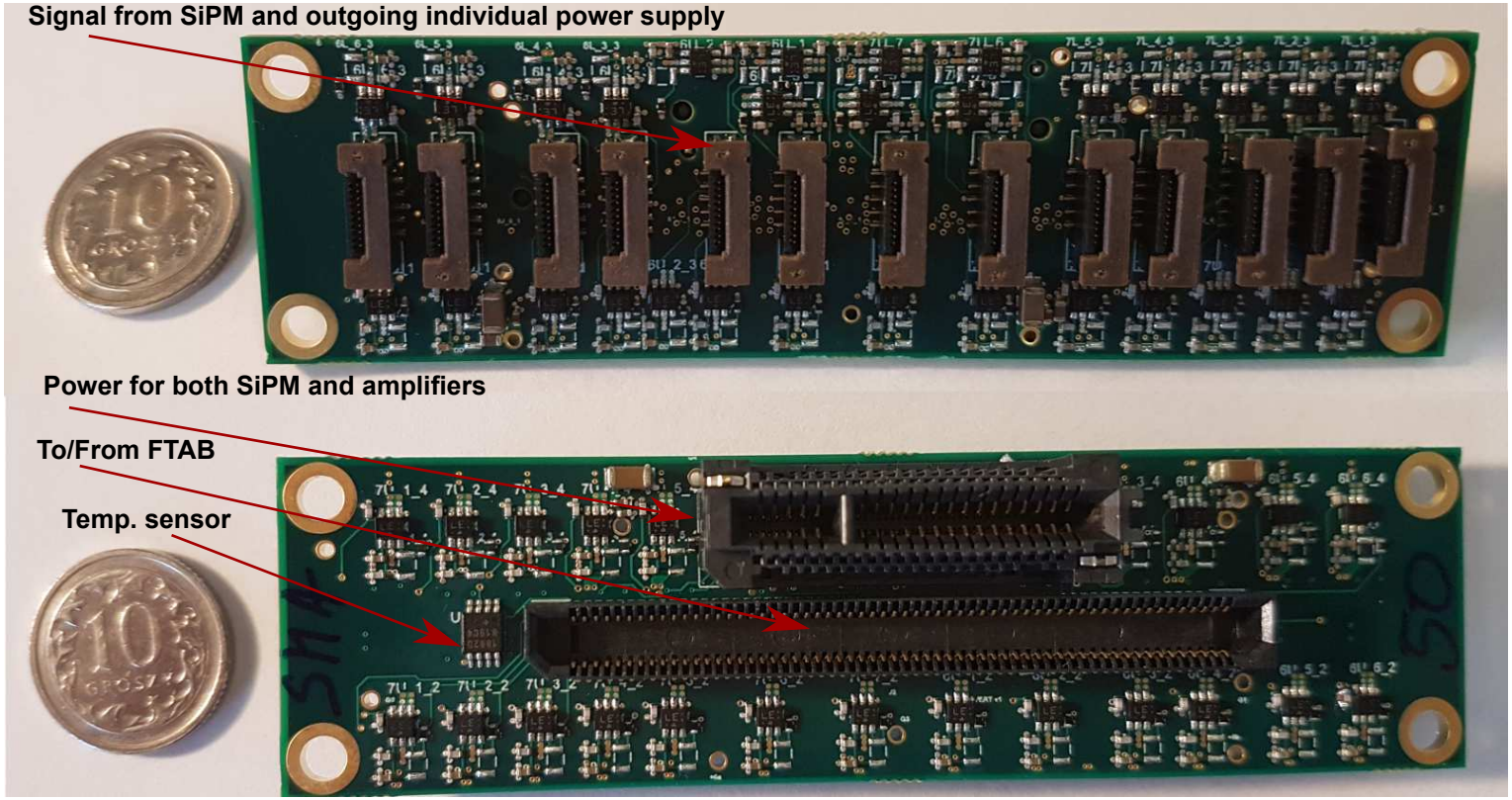

Fig. 2: Amplification stage

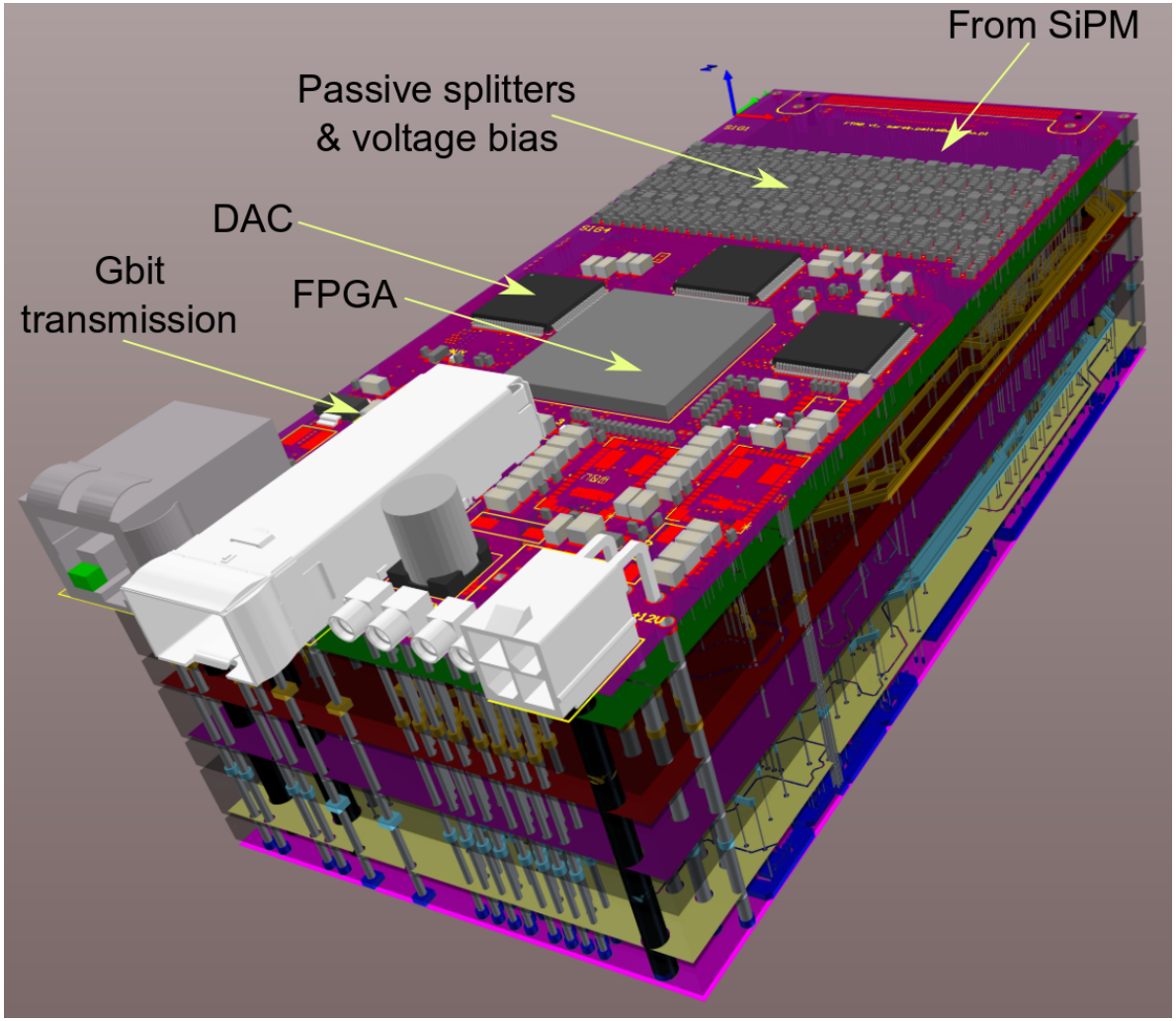

Fig. 3: FTAB PCB 3D view

PCB characteristics

- 1787 components
- 1185 nets (34377 tracks)
- 3134 vias
- only 16 × 7cm size
- 8 layers
- width and thickness of crucial paths are assuring low cross-talk
- tracks for SiPM signals have 50Ohm impedance (checked with manufacturer)

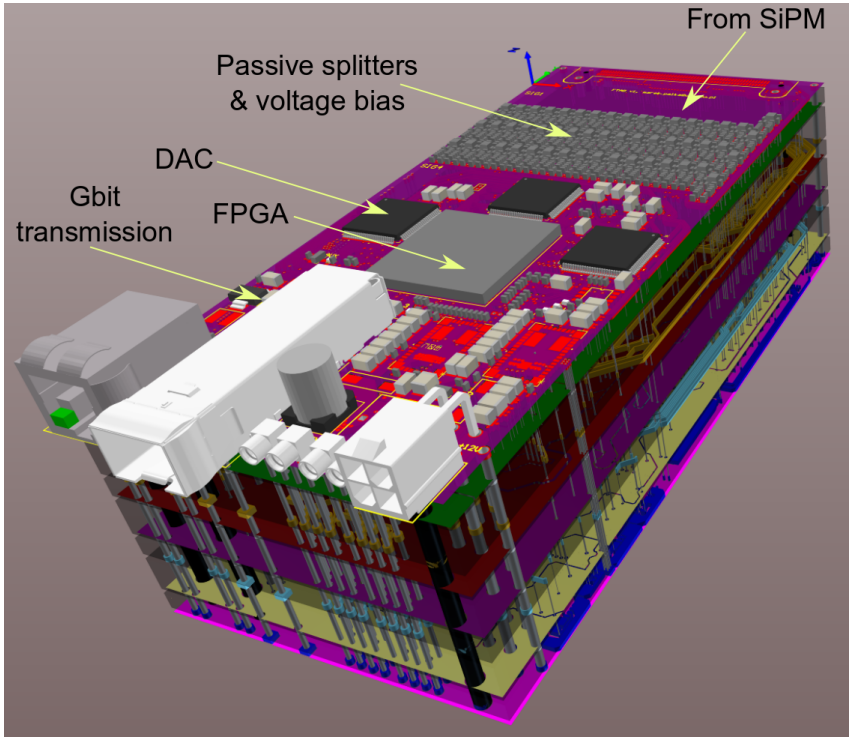

Fig. 4: FTAB PCB 3D view

Equipped components

- negative SiPM signals are adapted to be used by FPGA differential buffers (biased to 1024mV)
- the central place is taken by Artix7 200T FPGA, speed grade -2
- FPGAs differential buffers are used as comparators,
- three AD5381 40 channels, 12 bit precision DACs
- for connectivity purposes there are following interfaces:
  - Ethernet - stand alone operations
  - SFP - up to 6.4 Gbit
  - MMCX connector - up to 6.4 Gbit
- DC/DC converters - 5V, 3.3V, 2.5V, 1.8V, 1.2V, two times 1.0V

- low ripple voltage, well below Xilinx specifications, assures low intrinsic noise for SiPM signals and high TDC precision
- no problems with Gbit transmission at the maximum Artix7 rating
- stable DAC behaviour assured with careful schematics design
- voltage biasing with low pass filters to reduce cross talk

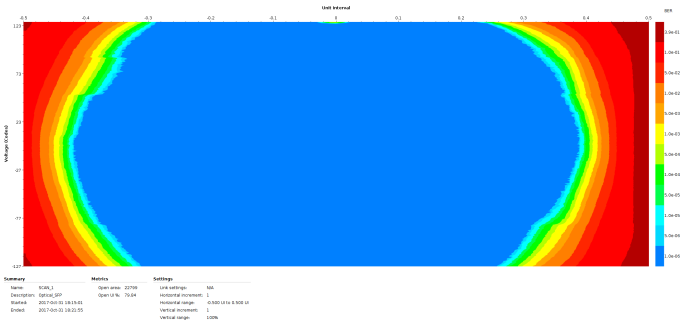

Fig. 5: Gbit transmission eye scan at 4Gbit/s

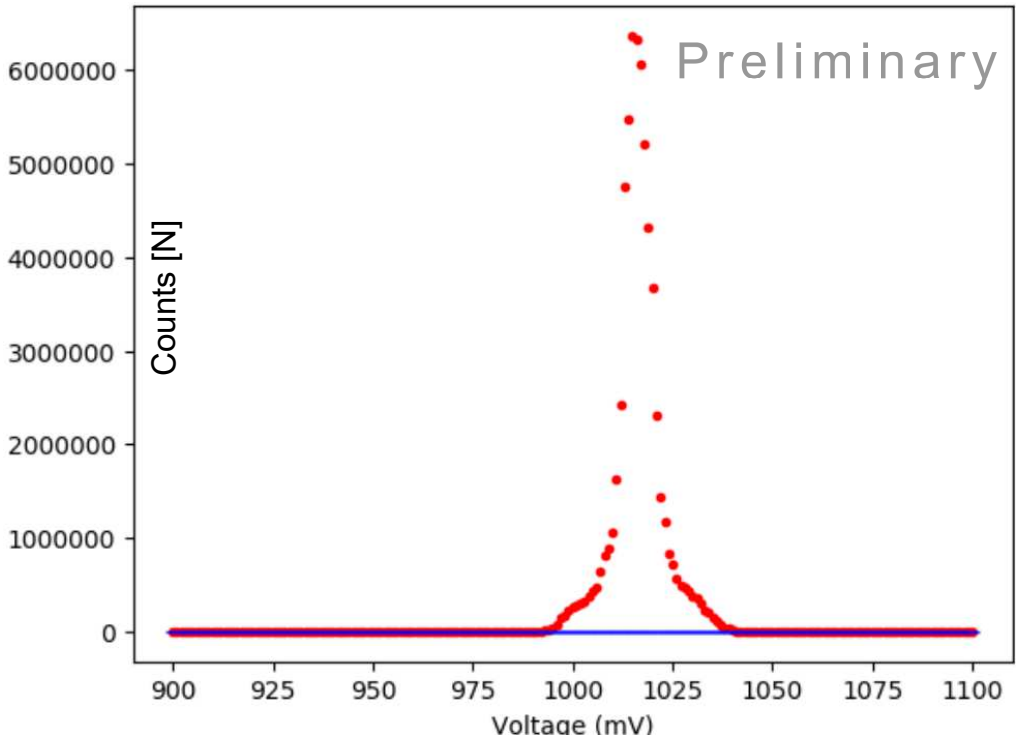

Fig. 6: Noise scan for one of the channels, bias voltage is at 1024mV

Using FPGA both as a multi channel TDC and comparator device allows to significantly reduce size and cost. It was possible to fit 105 TDC channels at 50% LUT and 35% FF usage. To ensure high TDC precision all these channels are placed "manually".

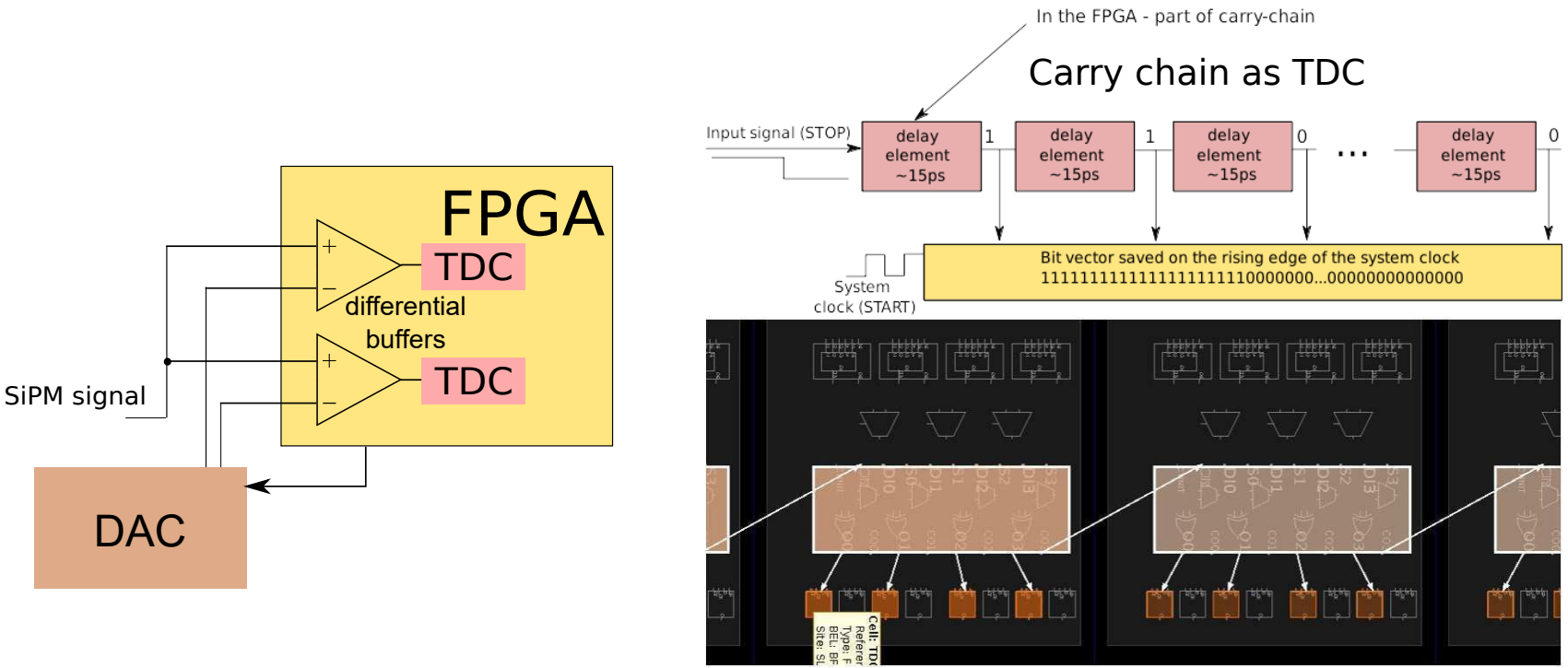

Fig. 7: FPGA differential buffers can be used for thresholding incoming signals which can be later sampled, at a given threshold, with TDC

- small form factor to fit into JPET modular design
- connected with SiPM power supply board and amplification stage
- amplifiers are proven to not heat up SiPM
- active air flow induced by small fan is sufficient to keep SiPM in room temperature

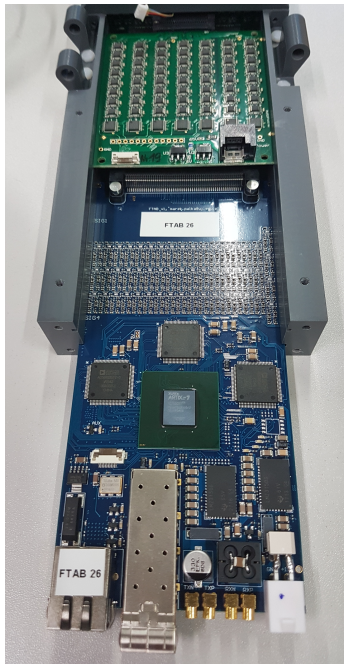

Fig. 8: FTAB with amplification stage (not visible) and power supplies (green board)

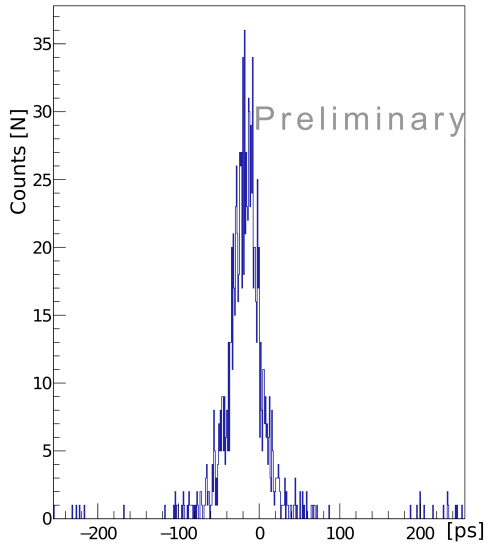

Fig. 9: Time difference between SiPM split signal, RMS $40ps$.

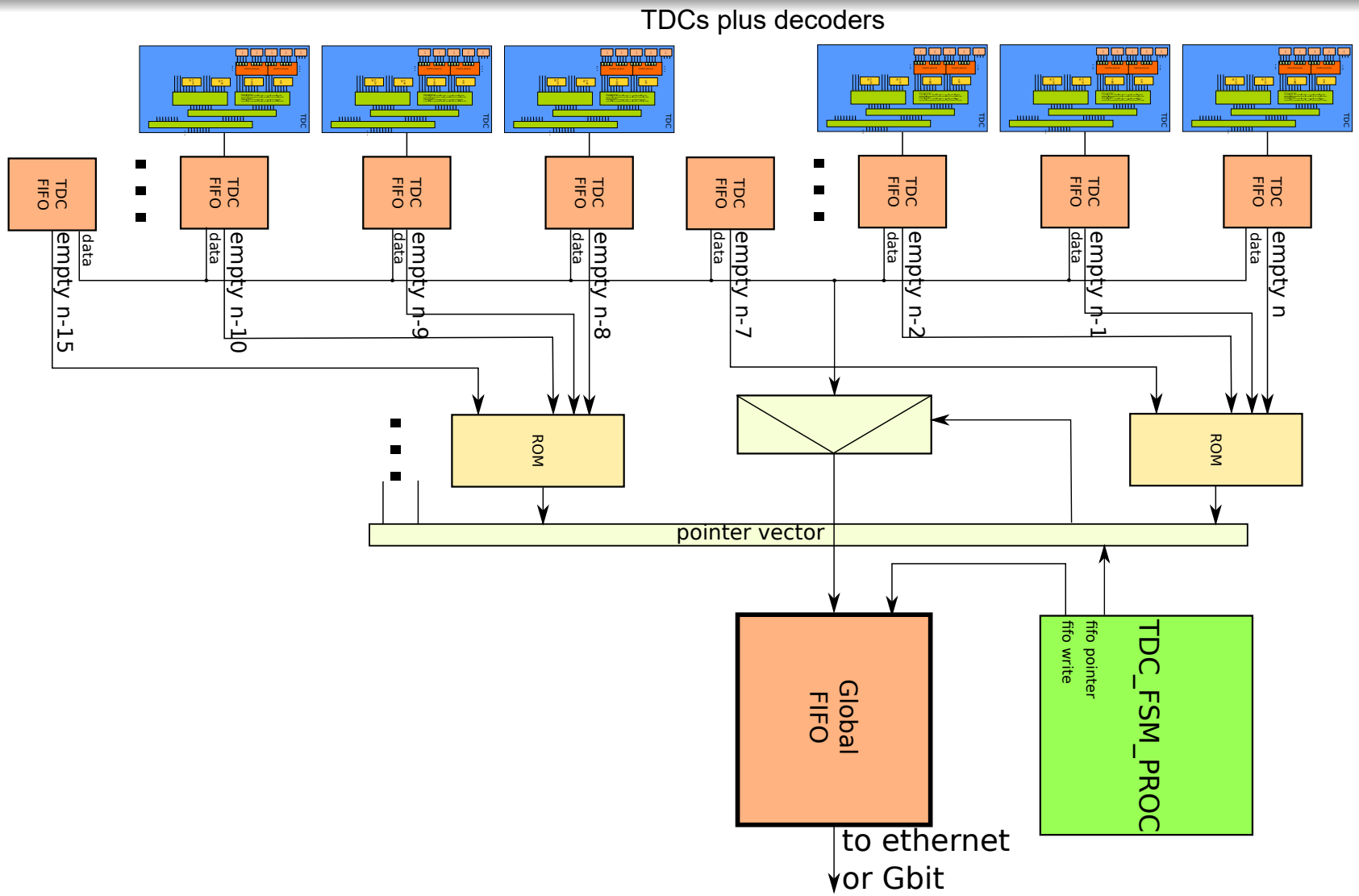

Fig. 10: Data is stored individually in TDC FIFOs. If one of the TDC FIFOs is not empty it is immediately read-out. To speed up read-out process fast algorithm is implemented (1 clock cycle) which gives list of pointers to not empty FIFOs. This significantly reduces dead time in the read-out

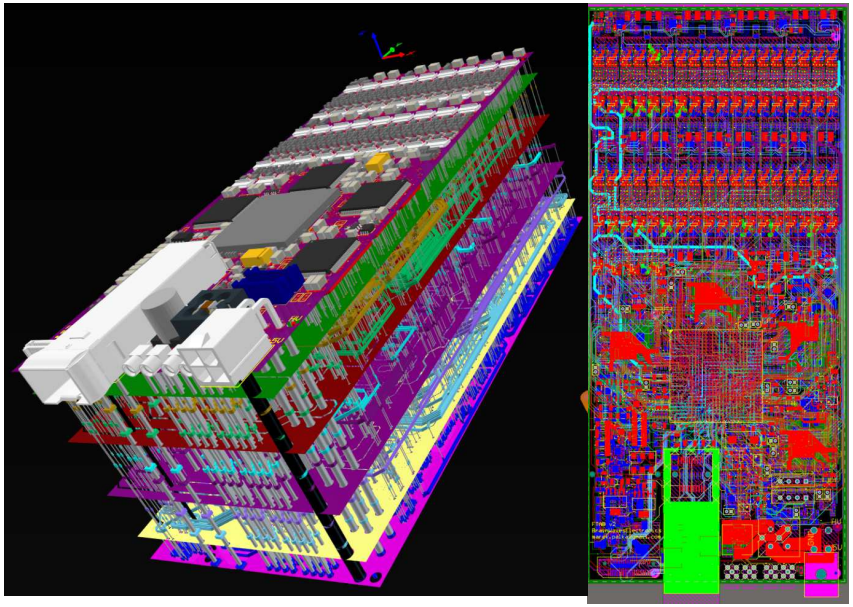

Fig. 11: New FTABv2 design is ready, it will incorporate 153 TDC channels, 4 DAC chips, integrated amplification and SiPM power supply stage.

FTABv2 PCB characteristics

- 3293 components
- 2034 nets (55810 tracks)
- 7550 vias
- only 16.5 × 7cm size
- 12 layers
- firmware can be directly adapted from FTABv1

Summary and Plans

- All the firmware has been written - its being tested/used
- Hardware undergoing tests
- FTAB will evolve
- FTABv2 will have also 152 ADC channels (implemented directly on the FPGA)
- Final price per amplification, thresholding, TDC, SiPM power supply, ADC and readout channel will be $\sim$ 20EUR
- FTAB can be used in other experiments